

Quality is more than a word



RELIABILITY FOR NEXT GENERATION SEMICONDUCTORS

Supporting the Future of Semiconductors

Environmental Test Solutions for Semiconductor Innovation

New Product Lineup

- 01 _Meeting Reliability Test Standards
- 02 _Supporting Miniaturization and Advanced Packaging
- 03 _Addressing Thermal Management and Heat Generation Challenges
- 04 _Supporting Mass Production and Automation

Reducing Energy Consumption in Standard
85°C/85%RH Testing

Temperature & Humidity Chamber

P.03

Supporting Tests Specifying a Temperature
Change Rate of 20°C/min

Thermal Cycle Test Chamber

P.03

HAST Chamber Supporting Testing
of Large Boards

Highly Accelerated Stress Test System (HAST)

P.04



Testing Standards

SOLUTION 01

Meeting Reliability Test Standards

Reliability test standards are essential for validating semiconductor device performance. Production environments require testing large sample volumes, while new device development demands support for evolving test requirements.

ESPEC provides environmental testing solutions that support industry-standard reliability testing and help streamline qualification for next-generation semiconductor technologies.

High-Precision Insulation Resistance and
Leakage Current Evaluation

Insulation Resistance/Leakage Current
Measurement System

P.05

Specialized for Low-Voltage Testing in 3D
Packaging and Redistribution Layers

Insulation Resistance/Leakage Current
Measurement System

P.05

Efficient Evaluation of Interconnect Reliability
Conductor Resistance Evaluation System

P.06

Specialized for Micro-Resistance Measurement
of Interposers and Redistribution Layers

Conductor Resistance Evaluation System

P.06

High-Temperature Electromigration Evaluation
for Advanced Interconnects

Electromigration Evaluation System

P.07



Miniaturization and Advanced Packaging

SOLUTION 02

Supporting Miniaturization and Advanced Packaging

Semiconductor technology continues to advance beyond the 2 nm node, accelerating the adoption of chiplets, 2.5D/3D packaging, advanced interposers, and complex RDL architectures.

As interconnects shrink and package complexity increases, evaluating electromigration, insulation degradation, and interconnect reliability demands greater precision. ESPEC provides measurement and evaluation solutions that help engineers validate and improve the reliability of advanced semiconductor packaging technologies.

Solu

Solutions for Four Critical

Thermal Management



SOLUTION 03

Addressing Thermal Management and Heat Generation Challenges

While the latest logic chips offer improved processing performance through higher integration and miniaturization, increased heat generation has become a challenge. Advanced thermal management is required as 3D packaging and chiplet technologies are adopted in practical applications. Demand for high-temperature operation is also expanding in the power semiconductor field, making thermal management an essential requirement.

Meeting High-Temperature Testing Requirements for SiC Power Devices

Thermal Shock Chamber Supporting 300°C High-Temperature Exposure

P.08

High Heat Load Capability for Next-Generation Semiconductor Devices

RBC Series Burn-In Chamber for High-Power Devices

P.08

Evaluating Degradation Under High Electric Field Stress

High-Temperature Reverse Bias (HTRB)/High-Humidity High-Temperature Reverse Bias (H3TRB) Test System

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Early Detection of Thermally Induced Failure Mechanisms

Power Cycle Test System

P.10

Identifying Thermal Design Bottlenecks Through Quantitative Analysis

Transient Thermal Resistance Measurement System

P.10

Temperature-Dependent Warpage Analysis for Advanced Packaging Materials

One-Device Temperature Test Chamber
Temperature-Dependent Warpage Measurement System and Analysis Services

P.11

Mass Production



SOLUTION 04

Supporting Mass Production and Automation

As new technologies advance toward practical application and mass production, new equipment is needed to support scale-up.

Heat Treatment for Advanced Packages

Slide-Tray Clean Oven
Anaerobic Clean Oven

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Mass-Production Heat Treatment Platform for the Organic/Glass Substrate Era

EFEM-Compatible Clean Oven System

P.13

Next-Generation Automation Without Compromising Batch Oven Performance

Batch Clean Oven Automation System

P.14

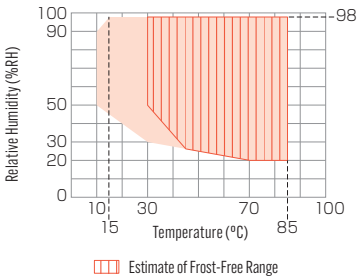
Reducing Energy Consumption in Standard 85°C/85%RH Testing



Temperature & Humidity Chamber Platinum J Series ECO Type

Supporting Semiconductor Reliability Test Standards

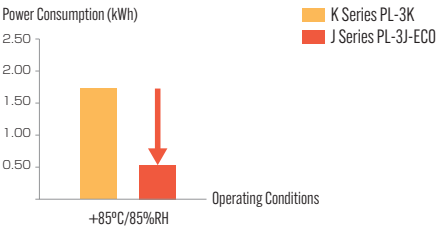
In addition to long-term continuous operation at 85°C/85%RH, this product delivers high energy-saving performance, especially in low-temperature ranges.



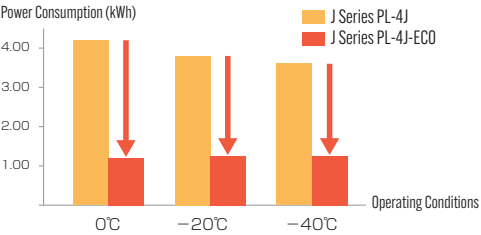
Low-GWP (Global Warming Potential)
R-449A Refrigerant Provided as
Standard



Power Consumption Comparison with Previous Products (Example) Per Hour



ECO Type Achieves Further Energy Savings in Negative Temperature Ranges



Specifications

Model		PL-2J-ECO	PL-3J-ECO	PL-4J-ECO
Temperature and Humidity Control System		Balanced Temperature and Humidity Control System (BTHC System)		
Performance	Temperature and Humidity Range	-40°C to +100°C (+150°C/+180°C with high-temperature control range expansion option installed)/20 to 98%RH		
	Time to Reach Extreme Temperature	Heat-up: +20°C to +100°C in 30 min		
		Cool-down: +20°C to -40°C in 45 min	Cool-down: +20°C to -40°C in 55 min	Cool-down: +20°C to -40°C in 115 min
	Temperature Change Rate	Temperature range: -26°C ↔ +86°C Heat-up rate: 3.0°C/min Cool-down rate: 2.0°C/min		Temperature range: -26°C ↔ +86°C Heat-up rate: 3.0°C/min Cool-down rate: 1.0°C/min

Supporting Tests Specifying a Temperature Change Rate of 20°C/min



Thermal Cycle Test Chamber Rapid-Rate Thermal Cycle Chamber

20°C/min Specimen Temperature Ramp

Fully supports JEDEC-specified specimen temperature ramp rate requirements

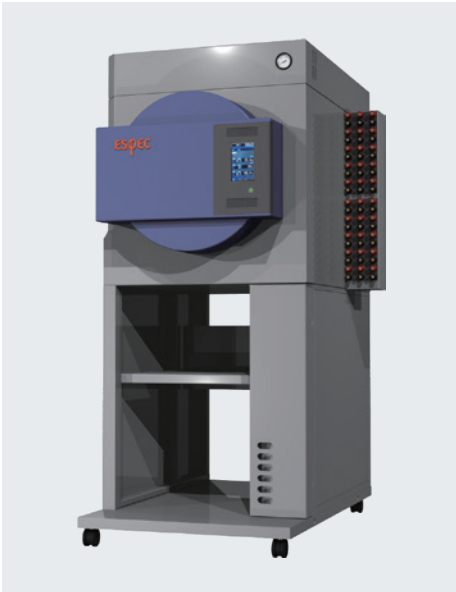
Supporting JEDEC/IPC Standards

Complies with the JESD22-A104 thermal cycle test method for semiconductor package reliability testing (15°C/min or less) and IPC-9701 for mounted board evaluation testing (20°C/min or less).

Specifications

Model	TCC-151W-20
Temperature Range	-70°C to +180°C
Temperature Change Rate	20°C/min *With 5 kg specimen (glass epoxy substrate) + 4 kg jig installed
Test Area Volume	160 L
Interior Dimensions/External Dimensions	W800 × H500 × D400 mm/W1000 × H1808 × D1913 mm

HAST Chamber Supporting Testing of Large Boards



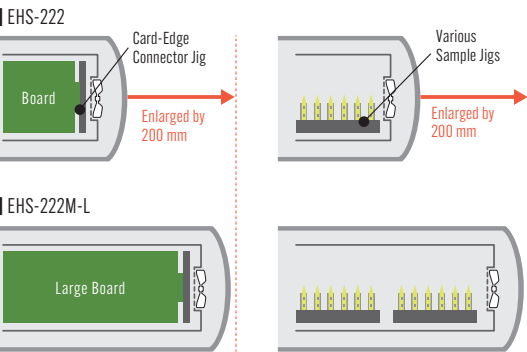
Highly Accelerated Stress Test System (HAST) Model for Large Boards and Large Sample Quantities

Supporting Standards Such as IEC 60068-2-66

ESPEC's proprietary dry- and wet-bulb temperature control function satisfies the test equipment conditions specified in IEC 60068-2-66 and enables the specified tests to be performed.
* ESPEC participated in and contributed to the establishment of IEC 60068-2-66.

Larger Chamber Depth × High Voltage × High Pin Count Compatibility Contributes to More Efficient Testing

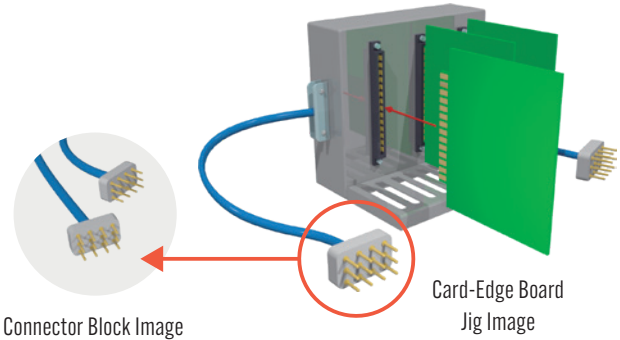
- Expanded depth
 - Supports large boards
 - Supports high voltage and high pin counts
- Interior dimensions: $\varnothing$ 394 mm × D626 mm
Can accommodate large boards up to 470 mm × 290 mm class
Enables energized testing at up to 1000 V and 1 A × 120 pins



Increasing the chamber interior dimensions enables large boards and large quantities of samples to be accommodated at one time, allowing statistically significant data to be obtained in a short period. This contributes to shorter development periods, lower testing costs, and shorter test cycles.

Also Reduces Test Preparation Time

Wiring work becomes more complex as the number of samples (pins) increases, but jig proposals using connector blocks simplify the process, thereby improving work efficiency and creating a stable test environment.



Specifications

Model	EHS-222M-L
Temperature and humidity range	+105.0 to +142.9°C / 75 to 100%RH
Pressure Range	0.019 to 0.193 MPa (Gauge)
Interior Volume	76 L
Interior Dimensions	$\varnothing$ 394 × D626 (604) mm *Dimensions in parentheses exclude fan guard protrusion.
External Dimensions	W1000 × H1713 × D1200 mm
Weight	310 kg
Heating/Pressurization Time (Unsaturated Control)	Within 70 min
Heating/Pressurization Time (Wet-Saturated Control)	Within 100 min
Heating/Pressurization Time (Dry- and Wet-Bulb Temperature Control/During Temperature Rise)	Within 90 min
Heating/Pressurization Time (Dry- and Wet-Bulb Temperature Control)	Within 130 min

High-Precision Insulation Resistance and Leakage Current Evaluation



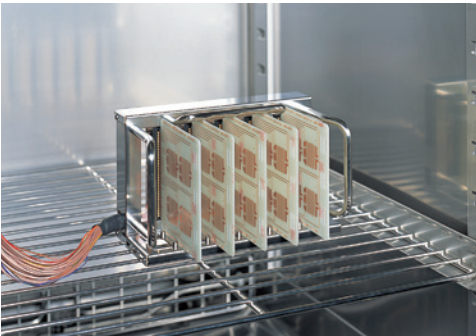
Insulation Resistance/Leakage Current Measurement System AMI

Insulation reliability has become increasingly critical as advanced packaging technologies, AI infrastructure, high-performance computing, and data center applications continue to evolve. The AMI system enables highly accurate, continuous monitoring of insulation resistance and leakage current across a wide range of test conditions. Designed for reliability evaluation of semiconductor packaging materials, substrates, electronic components, and power devices, AMI supports efficient detection of electrochemical migration and other insulation-related failure mechanisms.

Specifications: Stress Constant Voltage 100 V Specification

Resistance Measurement Range (Ω)	2.0×10^5 to 1.0×10^{13} (when applying 100 V) 2.0×10^3 to 1.0×10^{11} (when applying 1 V)
Measurement Voltage	1.0 to 100 V DC (0.1 V increments)
Leakage Current Detection Speed	Continuous detection in less than 100 μ sec

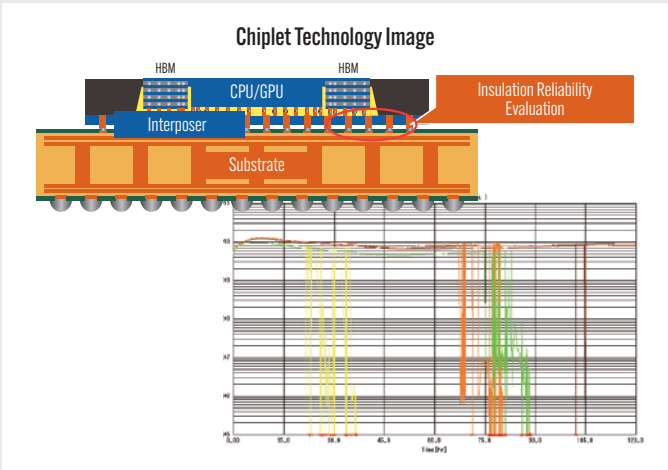
- [Test Purpose]** Insulation resistance/leakage current measurement, life evaluation, and insulation reliability evaluation of electronic components, substrates, semiconductor packaging materials, and power semiconductors
- [Supported Standards]** IPC-TM-650, IPC-B24, AEC-Q200, etc.
- [Test Functions]**
 - Automated multi-sample measurement and long-duration testing
 - Proprietary detection circuit enables detection of even momentary migration
 - Synchronization of resistance data and temperature/humidity data, and real-time failure analysis through integration with ESPEC chambers
 - Jigs: Dedicated jigs matched to samples reduce soldering work and connection errors



PREVIEW

Proposal for a New Insulation Resistance/Leakage Current Measurement System Specialized for Low Voltage in 3D Packaging and Redistribution Layers (New Materials)

Advanced packaging technologies such as chiplets, 2.5D/3D integration, and redistribution layer (RDL) architectures increasingly rely on new materials and finer interconnect geometries. As operating voltages decrease and packaging complexity increases, accurately evaluating insulation degradation under low-voltage stress becomes increasingly important. This system applies stress voltages below 1 V with 10 mV resolution, enabling highly sensitive insulation resistance evaluation for advanced semiconductor devices. Real-time life prediction analysis further supports faster reliability assessment and accelerated development cycles.



Efficient Evaluation of Interconnect Reliability



Conductor Resistance Evaluation System AMR

The AMR system continuously monitors low-level resistance changes in solder joints, package interconnects, and connector interfaces during thermal cycling. Automated data acquisition and analysis improve efficiency while enabling accurate reliability evaluation of critical electrical connections. When integrated with thermal cycling chambers, AMR provides a powerful platform for evaluating interconnect reliability in semiconductor packages, electronic assemblies, and advanced packaging technologies.

Specifications

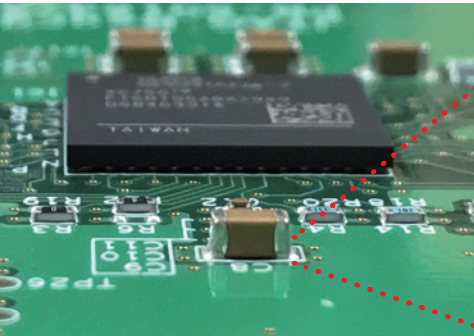
	Direct Electric Current Measurement System UD Type	Alternating Electric Current Measurement System UA Type
Channel Configuration	Standard 40 channels (max. 280 channels/rack)	
Measurement Interval	Within 12 sec for 40 channels (at 100 mΩ)	
Resistance Measurement Range	1×10^{-3} to $1 \times 10^8 \Omega$ (1 mΩ to 100 MΩ)	1×10^{-3} to $3 \times 10^3 \Omega$ (1 mΩ to 3 kΩ)
Measurement Accuracy	Within $\pm 1\%$ of true value when measuring 10 mΩ Within $\pm 0.5\%$ of true value when measuring 100 mΩ	Within $\pm 1\%$ of true value when measuring 10 mΩ Within $\pm 0.5\%$ of true value when measuring 100 mΩ
Measurement Range	10 mΩ, 100 mΩ, 1 Ω, 10 Ω, 100 Ω, 1 kΩ, 10 kΩ, 100 kΩ, 1 MΩ, 10 MΩ, 100 MΩ, and Auto	3 mΩ, 30 mΩ, 300 mΩ, 3 Ω, 30 Ω, 300 Ω, 3 kΩ, and Auto

- [Test Purpose]

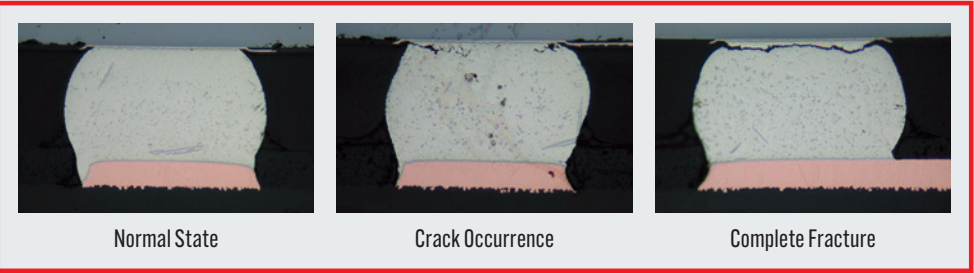
Joint reliability evaluation of packaging materials (boards, solder materials, conductive adhesives, etc.) and joint reliability evaluation of electronic components and chips
- [Supported Standards]

IPC-9701, etc.
- [Test Functions]

- Automates monitoring and data collection of conductor resistance (joint resistance) during thermal cycle tests, reducing measurement work and data variation
 - Uses measuring instruments that comply with international standards, enabling high-accuracy data acquisition
 - Automatically measures resistance change rates and absolute values, enabling failure judgment under user-selected conditions



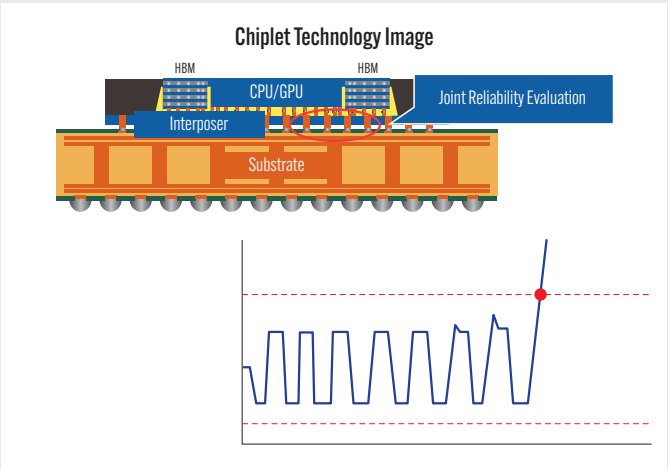
Progression of Solder Cracks



PREVIEW

Proposal for a Conductor Resistance Evaluation System Specialized for Micro-Resistance Measurement of Interposers and Redistribution Layers

As semiconductor packages become more complex, identifying degradation mechanisms before electrical failure occurs is increasingly important. Conventional pass/fail testing often provides limited visibility into how interconnects and package structures deteriorate over time. By continuously monitoring ultra-low resistance changes in the milliohm range and updating life prediction models throughout testing, this system enables earlier insight into degradation behavior, supporting more efficient reliability evaluation and development decisions.



High-Temperature Electromigration Evaluation for Advanced Interconnects



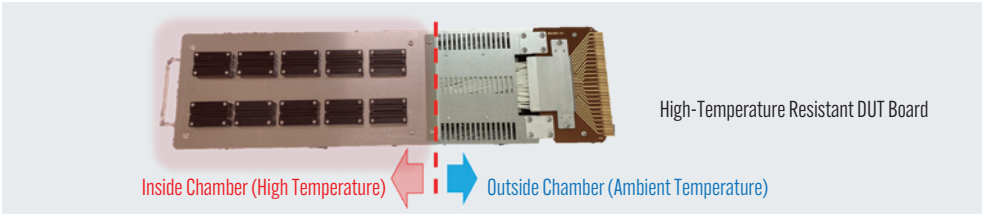
Electromigration Evaluation System AEM Series

Electromigration (EM) testing is used to evaluate the long-term reliability of semiconductor interconnects under accelerated stress conditions. The AEM Series applies precise current and temperature stress to multiple test structures simultaneously while continuously monitoring resistance changes and time-to-failure behavior. The resulting data supports lifetime prediction, materials evaluation, process optimization, and reliability qualification for next-generation semiconductor devices and advanced interconnect technologies.

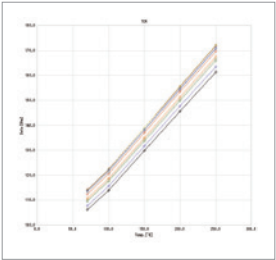
Specifications

Stress Current Source +DC/ -DC/ AC Specification	Output Range	$\pm(0.01 \text{ mA to } 50 \text{ mA})$
		$\pm(0.1 \text{ mA to } 200 \text{ mA})$
		$\pm(0.1 \text{ mA to } 500 \text{ mA})$
	Tracking Voltage	+33 V (+DC/AC)/-21 V (-DC/AC)
For Extrusion	Output Range	-20 V to +20 V
Oven	Temperature Control Range	(Ambient temperature +70)°C to +350°C
DUT Board	Number of Samples Mounted	10 DUTs/board (DIP 28-pin 600 mil, 300 mil)

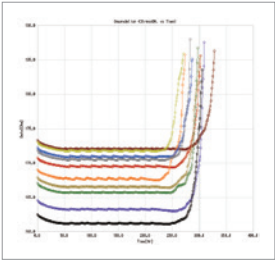
- Control up to three chambers and 300 measurement channels from a single system
- Select from three precision current source configurations: $\pm 50 \text{ mA}$, $\pm 200 \text{ mA}$, or $\pm 500 \text{ mA}$
- Independently configure test conditions in 10-channel groups for flexible test execution



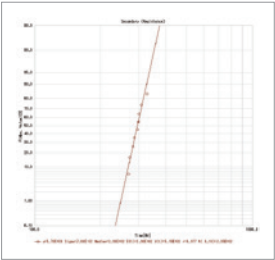
Integrated analysis software automatically calculates key reliability and lifetime prediction parameters from test data. Measured resistance values and derived reliability metrics are continuously updated and displayed in real time, allowing engineers to monitor degradation trends throughout the test.



Graphical display of resistance values by DUT and test temperature. Measured resistance values can be displayed by DUT and over time.



Display by relative change rate or absolute value. Secondary data calculated from the measured data can also be displayed graphically.



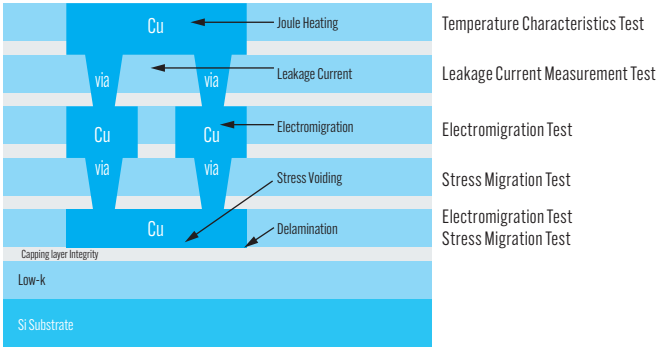
Normal probability plots and log-probability plots can also be displayed.

Supports Evaluation of Next-Generation Interconnect Materials

As AI and high-performance computing devices continue to drive interconnect scaling, alternative materials such as ruthenium and cobalt are receiving increased attention for their potential to improve electromigration resistance and overall reliability. To support evaluation of next-generation interconnect materials, the AEM platform can be configured for temperature stress testing up to 450°C and precision current sourcing from 0.1 nA to 50 mA, enabling advanced reliability characterization across a wide range of test conditions.

Reliability Evaluation of Cu Damascene Interconnect Structures

Cu damascene interconnect technology offers low electrical resistance and high performance, but the vias connecting multiple wiring layers remain susceptible to several thermally induced failure mechanisms throughout manufacturing and device operation. Understanding these failure mechanisms is essential for evaluating long-term interconnect reliability and predicting device lifetime.



Meeting High-Temperature Testing Requirements for SiC Power Devices



Thermal Shock Chamber Supporting 300°C High-Temperature Exposure

Supports the temperature-stress and thermal-shock testing required by ISO 26262 and IEC 61508.

Specifications Selectable by stationary specimen or elevator type, and chamber capacity.

			Stationary Specimen Type TSA-203ES-W (300°C Type)	Elevator Type TSD-101-W (300°C Type)	Elevator Type TSE-12-A (300°C Type)
Test Area	High-Temperature Exposure Temperature Range		+60 to +300°C		
	Low-Temperature Exposure Temperature Range		-70 to 0°C	-65 to 0°C	-65 to 0°C
	Temperature Fluctuation		±1.0°C	±0.5°C	±0.5°C
Temperature Recovery Performance	Conditions (Sensor Position: Upstream Side)	High-Temperature Exposure	+250°C, 60 min	+270°C, 40 min	+300°C, 30 min
		Low-Temperature Exposure	-40°C, 60 min	-40°C, 40 min	-45°C, 30 min
		Specimen	No specimen	Plastic-Molded IC 5 kg	Plastic-Molded IC 1 kg
		Temperature Recovery Time	Within 20 min	Within 5 min	Within 10 min
Test Area Interior Dimensions (mm)			W650 × H460 × D670	W710 × H345 × D410	W320 × H148 × D230
Capacity			200 L	100 L	11 L

PREVIEW High Heat Load Capability for Next-Generation Semiconductor Devices



RBC Series Burn-In Chamber for High-Power Devices

The RBC Series is designed for semiconductor reliability evaluation and high-volume burn-in screening. The growth of AI, high-performance computing, and advanced packaging technologies is driving significant increases in semiconductor device power density and thermal load. As advanced packaging technologies such as chiplets and 3D integration continue to increase device power density, thermal loads during burn-in testing are becoming significantly more demanding. The RBC Series combines high heat load capacity with uniform temperature performance to support evaluation of next-generation semiconductor devices. ESPEC is also expanding automation capabilities to accommodate increasing board sizes, device complexity, and higher pin-count configurations. To support future semiconductor packaging requirements, ESPEC is continuing to develop next-generation burn-in solutions that enable higher heat loads, larger burn-in boards, and greater test scalability.

- Main Specifications**
- Temperature Range: -10°C to +150°C
 - Burn-In Board Capacity: 24 boards (W450 mm × D570 mm)
 - Maximum Heat Load: 9 kW
 - High-Torque Automatic Burn-In Board Insertion/Removal System
 - Uses Low-GWP Refrigerant (R-449A)

* This product is currently under development, and specifications and appearance are subject to change without notice.

Evaluating Degradation Under High Electric Field Stress



High-Temperature Reverse Bias (HTRB)/High-Humidity High-Temperature Reverse Bias (H3TRB) Test System

Power semiconductor devices, including SiC-based technologies, are exposed to increasingly demanding operating conditions involving elevated temperatures and high electric field stress. These conditions can lead to increased leakage current, threshold voltage shift, and long-term degradation mechanisms that may ultimately affect device reliability in automotive, industrial, and infrastructure applications. To evaluate these failure mechanisms, reverse bias stress is applied under controlled temperature and humidity conditions while leakage current is continuously monitored. This approach enables early identification of insulation degradation, interface degradation, and other reliability risks before field failures occur.

[Test Purpose]

Long-term reliability evaluation of insulating films and interfaces in power semiconductors

[Supported Standards]

AQG-324 (automotive modules)/AEC-Q101 (automotive discretes)/JEITA ED-4701 (general semiconductors)

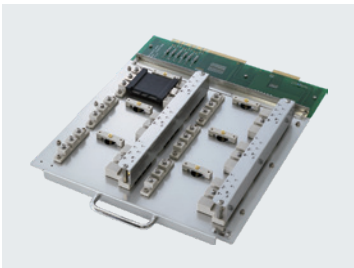
[Target Devices]

MOSFET/SiC/IGBT/Diodes, etc.

[Test Functions]

- **High-Temperature Reverse Bias (HTRB)**
Applies rated reverse bias voltage across an off-state device under elevated temperature conditions while continuously monitoring leakage current. Evaluates degradation of insulating films and electrical isolation between device terminals.
- **High-Temperature Gate Bias (HTGB)**
Applies gate bias under elevated temperature conditions near maximum junction temperature (T_j max) to evaluate gate oxide integrity, threshold voltage stability, and long-term device reliability.
- **High-Humidity High-Temperature Reverse Bias (H3TRB)**
Applies reverse bias under elevated temperature and humidity conditions, such as 85°C/85%RH, to accelerate moisture- and electric-field-induced degradation mechanisms, including increased leakage current and ion migration.

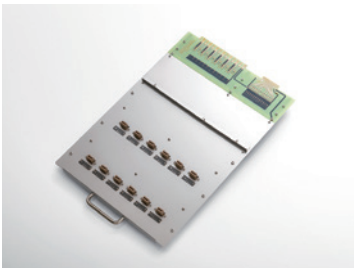
Example Test Boards



Board for 2-in-1 Modules
6 mounted/board
4 boards/chamber



Board for 6-in-1 Modules
2 mounted/board
4 boards/chamber

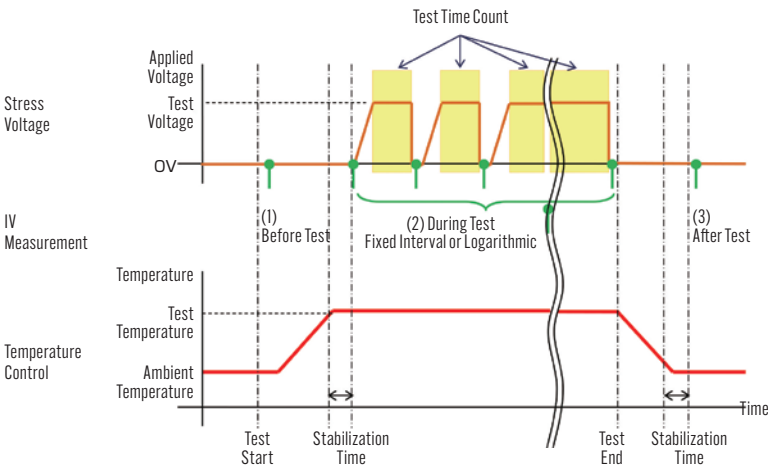


Board for TQ Packages
12 mounted/board
4 boards/chamber

Optional Function (I-V Characteristics Test: Evaluation of Threshold Voltage Variation)

[Temporarily stops applying stress during HTRB/HTGB testing and performs IV measurement]

- I_d-V_g (fixed V_d)/ I_d-V_d (fixed V_g) can be acquired. Characteristics variation during stress can be evaluated without removing specimens.
- $V_g \pm 30$ V and $V_d \pm 20$ V sweep settings allow confirmation of V_{th} drift, increased leakage current, and variation in on-resistance.



Early Detection of Thermally Induced Failure Mechanisms



Power Cycle Test System

As power semiconductor technologies continue to advance, managing thermally induced degradation remains a critical reliability challenge. Repeated heating and cooling cycles can lead to wire bond fatigue, interface cracking, solder degradation, and increasing thermal resistance, all of which directly impact device lifetime and package reliability. The Power Cycle Test System reproduces these operating conditions through controlled high-current loading and cooling cycles, enabling accelerated evaluation of failure mechanisms. By monitoring thermal resistance and package degradation throughout testing, engineers can identify reliability limitations earlier and improve device, package, and materials design.

Power Cycle Test

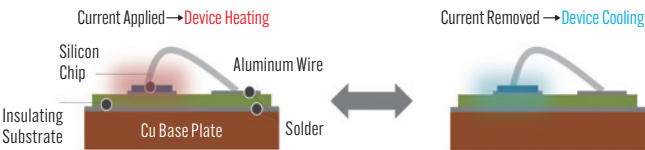
[Test Purpose] Long-Term Reliability Evaluation of Power Device Packaging Structures

[Supported Standards] AQG-324 (automotive modules)/
IEC 60749-34 (international standard)/
JEDEC JESD22-A105 (general semiconductors)

[Target Devices] MOSFET/SiC/IGBT, etc.

[Test Functions]

- **Temperature Characteristics Measurement**
Measures temperature characteristics of power transistors and obtains temperature coefficients α and β
* Measured within chiller temperature control range
- **Power Cycle Test**
Short Power Cycle/Long Power Cycle
- **Fixed Time**
ON/OFF Time
* Constant-current control/ T_{vj} free-run control
- **Temperature Target**
Fixed Maximum and Minimum Junction Temperature (ΔT_{vj}) Testing
* Select stress current control and ON time control
- **Transient Thermal Resistance Measurement Function (Option)**
* This option is available only in Japan.



Identifying Thermal Design Bottlenecks Through Quantitative Analysis

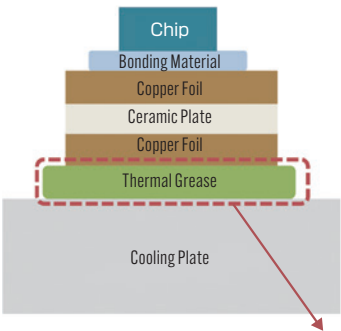


Transient Thermal Resistance Measurement System

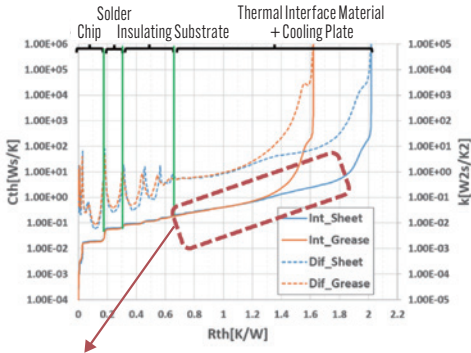
*This product is available only in Japan.

Power devices used in automotive, data center, industrial, and infrastructure applications continue to face increasing thermal management challenges. Insufficient heat dissipation can lead to localized hot spots, interface degradation, increased thermal resistance, and ultimately reduced device reliability.

[Evaluation Sample Image]



[Structure Function Graph (TIM Material Comparison)]

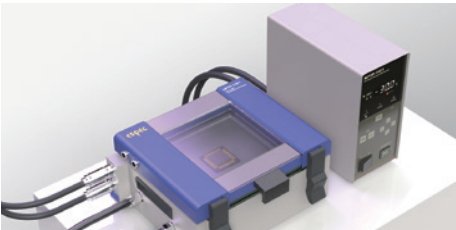


Comparison of Heat-Dissipating Silicone Pad (TC-50TXE) and Grease (SCH-20)
Differences in thermal interface material performance can be clearly identified through structure function analysis. The resulting data helps engineers isolate thermal resistance contributions and evaluate the impact of material selection on overall thermal performance.

Thermal-Dependent Warpage Analysis for Advanced Packaging Materials and Electronic Assemblies

One-Device Temperature Test Chamber

*This product is available only in Japan.



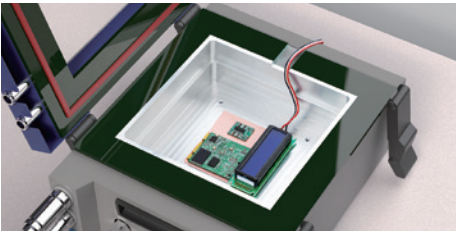
The One-Device Temperature Test Chamber provides a stable, windless temperature environment from -30°C* to +150°C in a compact tabletop design. Its low-disturbance thermal environment makes it well suited for electrical measurements, optical observations, and material characterization under controlled temperature conditions. A large observation window and PC-based control software enable convenient monitoring, data collection, and programmable test operation. The system can also be integrated with optical measurement equipment and specialized analysis tools.

*Temperatures down to -40°C can be achieved when using antifreeze in the cooling water circulation system.

Temperature-Dependent Warpage Measurement System and Analysis Services

*This product is available only in Japan.

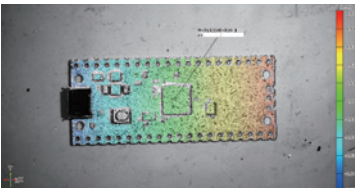
Visualizes Temperature-Dependent Warpage and Surface-Temperature Distribution of Mounted Boards Under Controlled Temperature Conditions



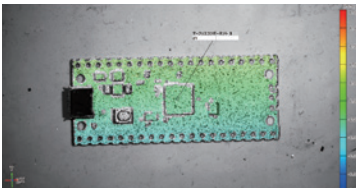
Visualizes temperature-dependent warpage, strain distribution, and surface-temperature behavior under actual operating conditions. By combining a 3D Digital Image Correlation (3D DIC) system with ESPEC's dedicated thermal chamber technology, engineers can evaluate displacement, strain distribution, and coefficient of thermal expansion (CTE) across a temperature range of -40°C to +260°C. When integrated with thermal imaging, the system enables simultaneous non-contact measurement of deformation, strain, and surface temperature distribution, providing deeper insight into package and assembly behavior during thermal exposure.

- High-resolution strain mapping supports package and board design validation.
- Measures displacement with accuracy at the 1 μm level.(field of view: W20 × D15 × H4 mm).
- Measured temperature and deformation data can be incorporated into CAE models to improve simulation accuracy and correlation with physical test results.

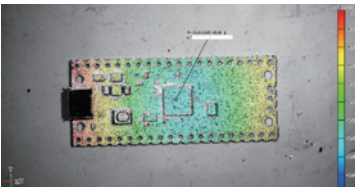
Temperature-Dependent Warpage Measurement Example



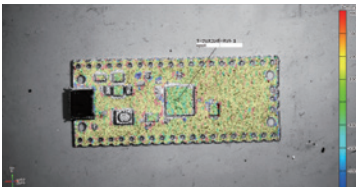
(125°C X-Direction Displacement)



(125°C Y-Direction Displacement)



(125°C Z-Direction Displacement)



(125°C X-Direction Strain)



Temperature-Dependent Warpage Measurement System 3D DIC + One-Device Temperature Test Chamber

Supports evaluation of thermal warpage in semiconductor packages and electronic assemblies while improving the accuracy of simulation and reliability analysis.

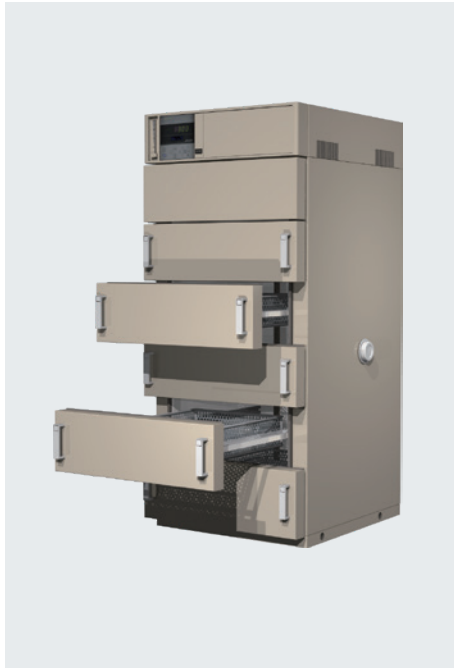
CAE Model Validation Using Measured Temperature-Dependent Warpage and Thermal Imaging Data

[Comparison of Measured Temperature-Dependent Warpage Values and CAE Analysis Results]

CAE analysis results provided by: Cybernet Systems Co., Ltd.

Temperature Conditions		Measured Thermal Dependent Warpage Values	CAE Analysis Results			
			Analysis Results Before Correction	Step 1 Add Surface Insulating Film Conditions	Step 2 Add Measured Surface Temperature Distribution Values	Step 3 Add Viscoelastic Conditions
+125°C	Warpage Deformation Diagram					
	Warpage Amount	+136.0 μm	-39.9 μm	+27.8 μm	+90.6 μm	+153.1 μm
	Match Rate	—	-29%	20%	67%	113%

Heat Treatment for Advanced Packages



Slide-Tray Clean Oven

The slide-tray design enables independent thermal processing at each access door, eliminating the need to accumulate work-in-process before loading. This allows materials to move directly to downstream processes without unnecessary waiting time.

By minimizing temperature loss during loading and unloading operations and enabling rapid temperature recovery, the system improves equipment utilization, increases throughput, and supports more efficient thermal processing operations.

High Cleanliness: ISO Class 5

Achieves ISO Class 5 cleanliness through front-flow air circulation and HEPA filtration.

Designed for baking, drying, and thermal processing applications requiring clean-air environments, the system combines a compact vertical footprint with enhanced operational safety. Interactive control options simplify operation, while a high-temperature HEPA filtration option maintains stable cleanliness performance at temperatures exceeding 150°C.

Specifications

Temperature Range	(Ambient temperature +20°C) to +120°C	
Number of Sliding Tray Levels	4 levels	5 levels
Effective Sliding Tray Dimensions	W660 × H200 × D700 mm	W438 × H140 × D492 mm
Load Capacity per Tray Level	20 kg	20 kg



Anaerobic Clean Oven SCO Series

As integration density and processing speeds increase, advanced packaging technologies such as “2.xD” packaging are attracting growing attention. In this process, precise heat treatment is essential, from interposer formation to post-packaging annealing.

Features

- High-temperature thermal processing up to 500°C
- Oxygen concentration control to 10 ppm or less
- Stable ISO Class 4 cleanliness
- Real-time monitoring and data logging of temperature, oxygen concentration, and process parameters
- Support for automation, host communication, and GEM integration

Specifications

Model	SCO-2 Type	SCO-3 Type	SCO-4 Type
Interior Dimensions	W600 × H700 × D700 mm	W750 × H800 × D850 mm	W900 × H950 × D1000 mm
External Dimensions	W1400 × H1760 × D2090 mm	W1550 × H1910 × D2240 mm	W1710 × H2000 × D2510 mm
Recommended Workpiece	300 mm wafer	510 × 515 mm/600 mm square substrate	Multiple processing
Temperature Range	+80°C to +350°C (OP: supports +50°C to +500°C)		
Chamber Cleanliness	Class 5 at all times (Option: Class 4)		
Oxygen Concentration	100 ppm or less (Option: 10 ppm or less)		
Options	Automation support, host communication support, GEM communication support, etc.		

Mass-Production Heat Treatment Platform for the Organic/Glass Substrate Era



EFEM-Compatible Clean Oven System

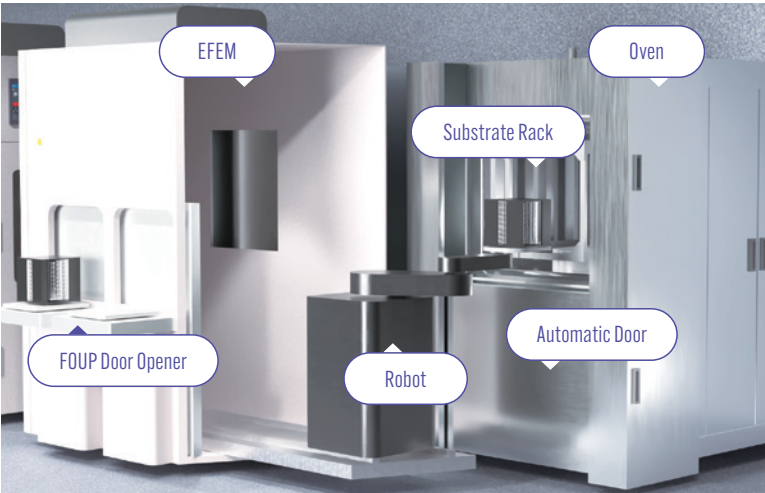
As advanced packaging technologies continue to evolve, precise thermal processing is required throughout the manufacturing flow, from interposer fabrication through assembly, encapsulation, and final package processing.

At the same time, the industry is transitioning from traditional silicon wafer manufacturing toward larger organic and glass substrate platforms. Supporting these larger-format substrates requires improved thermal process control, faster throughput, and higher levels of automation.

The EFEM-Compatible Clean Oven System provides a scalable thermal processing platform designed to support high-quality, high-volume manufacturing of next-generation semiconductor packages.

Features

- Supports large panels up to 600 × 600 mm
- Provides high cleanliness levels and precise temperature uniformity control.
- Proprietary cooling mechanism significantly reduces temperature recovery time while maintaining a low-oxygen state
- Supports system configurations tailored to substrate size, production requirements, and throughput objectives. ESPEC provides integrated solutions that include automated material handling, host communication interfaces, and compliance with semiconductor automation standards such as GEM300.



Specifications

Supported Substrate Size Examples	300 mm × 300 mm, 515 mm × 510 mm, 600 mm × 600 mm, etc.
System Configuration	Oven × 2 chambers + automatic transport system (loader × 2 ports/unloader × 2 ports)
Typical Capacity	24 substrates/cassette (total processing of 48 substrates)
Temperature Range	+80°C to +350°C
Chamber Cleanliness	Class 5
Residual Oxygen Concentration	100 ppm or less
Supported Standards	MES-compatible/GEM300-compliant

* The above specifications are examples. Please contact us for details.

Next-Generation Automation Without Compromising Batch Oven Performance



Batch Clean Oven Automation System

Growing automation needs in semiconductor back-end manufacturing. ESPEC’s Batch Clean Oven Automation System enables automated thermal processing while preserving existing thermal characteristics.

This approach helps accelerate production ramp-up while minimizing process disruption and requalification efforts. Batch ovens are widely used for post-bake, pre-bake, annealing, and other semiconductor thermal processing applications. By integrating automation without altering established thermal process performance, manufacturers can improve throughput, reduce manual handling, and support a faster transition to volume production.

Supports Low-Oxygen Processing and Shorter Cycle Times in Semiconductor Manufacturing

Supports key semiconductor manufacturing requirements, including low-oxygen processing environments and reduced cycle times. Features such as oxygen concentration control and accelerated cooling help optimize thermal processes while maintaining product quality and process consistency.

Communicates with Host PCs and Automated Transport Systems, Including AGVs and AMRs

Supports integration with factory automation systems, including host communication platforms, AGVs, AMRs, mobile manipulators, and automated material handling equipment. The system can coordinate automated door operation, workpiece loading and unloading, process data collection, and communication with upstream and downstream manufacturing processes.

Specifications

System	Forced hot-air circulation and ventilation system
Temperature Performance	RT +60°C to +200°C
Interior Dimensions	W800 × H1000 × D700 mm
External Dimensions	W2300 × H2200 × D1500 mm *Excluding protrusions
Automatic Door	Left-right sliding automatic door specification
Nitrogen Gas Supply Device (Pressure/Flow Rate)	0.5 to 1.0 MPa, 300 NL/min
Cooling Function (Pressure/Flow Rate)	0.3 to 0.7 MPa, 10 L/min
Communication Function/Transport Mechanism	Host communication and integration with automated material handling systems
Pressure Relief Port Nitrogen Gas Exhaust	Operation panel
Operation Panel	Touch panel LCD
Power Supply	200 V AC, 3 φ, 50/60 Hz
Air	Compressed air

* The above specifications are examples. Please contact us for details.
Products handled by ESPEC Thermal Tech System Co., Ltd.

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