Quality is more than a word





"Thermal management" is the Key for the future of semiconductors.

Advanced Semiconductor Testing Equipment

The high-speed processing and advanced functionality of semiconductors significantly impact thermal design challenges. "Thermal management in semiconductors is essential for performance enhancement, reliability assurance, and product longevity." ESPEC proposes and supports optimal evaluation methods for semiconductor assessment in thermal management.

Process	Front-end process	Back-en	d process	Inspection
Techno	Development of leading-edge processes of 2 nm level.	 Chiplet and heterogeneous technology Advanced 2.xD 3D package Interposer Chip stacking technology Low-K materials GPU GPU HBM 		The screening process and final inspection
Technology trend	<list-item><list-item><list-item><list-item><list-item><list-item><list-item></list-item></list-item></list-item></list-item></list-item></list-item></list-item>			 Inspection for advanced the 2nm process Chiplet implementation inspection process Inspection methods for each chiplet implementing process
Quality trend	Issues of advanced process operations, quality evaluation at the wafer level	Quality of the fine implementation process int middle-end process		Yield improvement of advanced devices
	<text></text>	 Finer redistribution layers and TSV connection Affect of local heat generation of chips Quality of the fine implementation process int middle-end process 		 Process inspection in the front-end process Process inspection in the middle-end process Process inspection in the back-end process Burn-in test for Advanced Semiconductor
Our proposal products	Wafer level semiconductor characteristics evaluation equipment	High-performance, Anaerobic Clean Oven	Package level semiconductor characteristics evaluation equipment	Burn-in test products
	Semiconductor Parametric (Wafer Level) AMM Series TDDB Evaluation System (Wafer Level) AMM Series	SCO Series PVHC Series	 Semiconductor Parametric test system (Package Level) AMM Series TDDB Evaluation System SMU Type (Package Level) AMM Series 	 Static Burn-In System Dynamic Burn-In System
	https://www.espec.co.jp/english/ products/measure-semicon/tddb/	https://www. espec.co.jp/english/ products/env-test/sco/	espec.co.jp/english/ products/measure- semicon/spa/	https://www.espec.co.jp/english/ products/measure-semicon/rbs/
	This equipment evaluates process defects in the wafer process using parameter testing in combination with a full-auto prober.	Mitigate the devices in high temperature environment required for polyimide to imidize (400°C or more) by providing an ultra-low oxygen atmosphere. Uniform insulating layer film can be formed by heat treatment with high temperature distribution performance.	This equipment tests semiconductor parameters to verify process issues after packaging. With a temperature chamber, transistor characteristics can be evaluated at the package level in real time under a constant temperature environment.	As part of burn-in tests, there is a process to screen defective advanced devices such as SoCs and GPUs. Products being tested are subjected to voltage load or input signals at high temperatures to find and select potentially defective devices before shipping. This equipment integrates the above as an all-in-one testing system with a temperature chamber and has been delivered to many customers.
Standard	-	-	_	_
CE	_	-	-	_







Phenomenon of electrochemical migration (lon migration)



Microcracks at a joint

Compliance with semiconductor test standards JEITA ED4701/001A

JEITA ED4701/100A

Test method 102A: High-temperature, high-humidity bias test Test method 103A: High-temperature, high-humidity storage test Test method 104A: Humidification + Packaging stress series test Test method 105A: Thermal cycle test

JEITA ED4701/200A

Test method 201A: High-temperature storage test Test method 202A: Low-temperature storage test (reference test) Test method 203A: Temperature and humidity cycle test (reference test)

Thermal shock chamber Semiconductor me		asurement systems	HALT, HASS	One-device, spot heating and cooling
Conductor Resistance Eval	uation System (AMR Series)	 Electro-Migration Evaluation 	♦ Typhoon Series	♦ MTA Series
 TSA Series TSD Series TSB Series 	 Conductor Resistance Evaluation System (AMR Series) 	System (AĔM Series)		
https://www. espec.co.jp/english/ products/catalog/ tsa.pdf	https://www. espec.co.jp/english/ products/catalog/ amr.pdf	https://www.espec.co.jp/ english/products/ measure-semicon/aem/	https://espec.com/ na/products/#halt	https://www. espec.co.jp/products/ env-test/mta/ (Japanese only)
Thermal shock chambers are designed for reliability testing by accelerating deterioration, such as cracks at joints, by instantaneously switching between high and low temperatures. Elevator-type and the liquid-to-liquid thermal shock type chambers are also available.	Microcrack in joints and other connection defects cause conduction failures only when the temperature rapidly changes. With a thermal shock chamber, the Conductor Resistance Evaluation System can capture conductor resistance in real time in a controlled temperature environment, allowing for quick and accurate evaluation of connection reliability.	Electromigration evaluation tests assess the lifespan of semiconductor interconnects by applying optimal current density and temperature for accelerated testing. Accelerated testing can also be performed at high temperatures at 450°C.	Performing HALT at an initial stage of the product development process can improve product reliability. This series also supports HASS.	The Spot Cooling and Heating System is a chamber-free system where specimens are cooled and heated by air sprayed by a hose. The front heater type changes air temperature by 100°C/min, allowing for significant reductions in testing time.
MIL-STD-883L IEC60068-2-14Na, ED-2531BNa	_	_	-	-
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Modification of Environmental Test Chamber for Semiconductor market





Sliding Panel-Mounted Terminal Blocks

Sample holder type

Removable Terminal Blocks



Simple wiring + simple installation = reduced work time

https://espec.satori.site/ products/catalog/ usability#sec6

(Japanese only)



https://www.espec.co.jp/ english/products/book/ hast/#target/page_no=13



Flat cable port type

Terminal block allows 12-pin specimen signal terminals in the test area to be inserted and removed at once



Applicable Series

HAST Chamber

Terminal block that slides to the front

Semiconductor Heat Treatment System







Ideal for low oxygen annealing required for 3D semiconductor packaging and integration.

Enables heat treatment at the lowest oxygen concentration of 10 ppm (0.001%) and Class 5 cleanliness.

• Handles low oxygen, high-temperature annealing from 350 to 500°C. Reduced process time by water cooling.



https://www.espec.co.jp/ english/products/ env-test/sco/



Large Highly Accelerated Stress Test System-HAST Chamber







Rapid-Rate Thermal Cycle Chamber



Applicable Series

RBS-PST

Self-heating cycles due to current on/off

disconnection and destruction of heat

dissipation circuits. Power cycle tests are

conducted to improve product reliability.

setting temperature.

Cycle mode Repeat "Ice" ON/OFF by setting the time.

Control the temperature and volume of

temperature setting while "Ice" is constant.

Repeat the control of "Ice" ON/OFF for

specimen temperature to achieve the

cooling water to achieve the device

of power devices cause wiring

Major test modes

Continuous

mode

Vf cycle

mode

Power Semiconductor-Related Equipment



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