

Latest trends in wafer level burn-in systems

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Wafer Level Burn-In (WLBI) has been an extremely effective measure for guaranteeing Known Good Die (KGD) and reducing ever-expanding testing costs. The industry has very high interest in the method. This article will discuss the latest trends in wafer level burn-in and look at newly-developed equipment capable of simultaneously burning in 256 die, four times the previous processing capacity.

1. Introduction

Burn-in technology is becoming increasingly important as a quality assurance measure that can aid in adopting new materials, assuring new miniaturization technologies such as CSP (Chip Size Package*¹), and developing processing technology more rapidly. On the other hand, expensive test equipment has become necessary for LSI (Large Scale Integrated circuits), which are advancing toward accelerated speed and higher-level functions. Expanding memory capacity also places heavier demands on test time, and these twin factors of expensive equipment and increased test time have been pushing up testing costs.

Radical reform of cost structure itself is seen as essential in such areas as cutting test costs by adopting DFT (Design for Test) technology, lowering production costs in wafer processes, and increasing yield.

Demands for miniaturization, lower weight, and higher functionality in items such as car electronics and all types of portable devices has generated interest in bare chip packages*² such as stack type CSP and MCP*³. This has led to a high demand for a supply of KGD with burn-in screening completed and quality and reliability verified, and so currently strong efforts are being concentrated in this area.

At present, there are high hopes for resolving the difficulties regarding the reliable supply of KGD and the reduction of test costs by performing Wafer Level Burn-In, known as WLBI.

The recently developed wafer level burn-in system WBD-03 now has four times the burn-in capacity of conventional systems, raising the number of simultaneous burn-in capability from 64 die to 256 die. This system achieves optimum cost performance using the partition contact method, stirring further anticipation that WLBI will resolve the above-mentioned difficulties.

2. Successful introduction of WLBI

The adoption of WLBI holds the key to solving the thorny problem of reducing test costs by using package burn-in, while also guaranteeing KGD.

(1) Reducing burn-in boards

The increasing use of higher numbers of pins has resulted in larger sockets, reducing the number of devices that can be mounted on a burn-in board. Also, greater diversity in package types has led to a corresponding diversity in the types of burn-in boards. These factors have led to rising manufacturing costs for burn-in boards. Other problems affecting the industry include rising unit costs, development costs for IC sockets, and problems with contact reliability.

The amount of money invested in burn-in boards has been said to equal that of the test equipment, but recently, the cost of the boards has been accounting for an increasingly large share of investment funds, and this is one factor in driving up overall test costs.

However, as WLBI contactor is not affected by package specifications, only one type of WLBI needs to be developed per device, offering yet another means of reducing costs.

(2) Reducing burn-in time

Increased functionality and higher levels of integration have brought a corresponding increase in burn-in time, producing the need to increase the amount of test equipment that must be installed and thus driving up test costs. Incorporating test technology into the chip itself, such as BIST (Build In Self Test) which includes the burn-in circuits in the chip using the DFT approach, has been crucial to reducing costs. Fig. 1 shows the necessity of BIST introduction.

Using the WLBI partition contact method, a unique burn-in BIST is created inside the chip, and burn-in can be performed efficiently in less time by directly contacting this circuit's pad (electrode on the wafer) for control.

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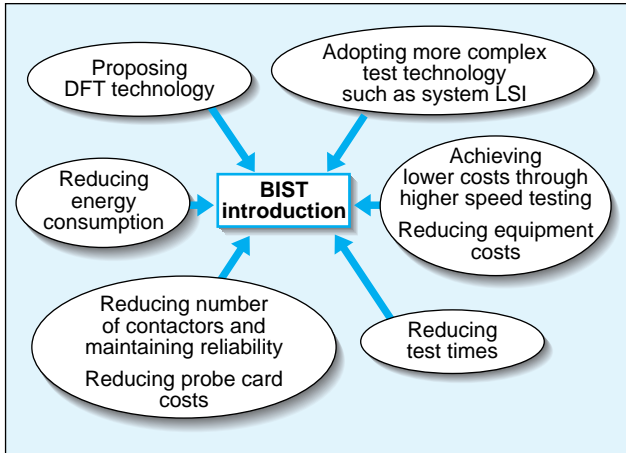


Fig. 1 Necessity of BIST introduction

Table 1 shows a comparative chart of processing quantity and investment efficiency for WLBI equipment and package burn-in equipment. BIST adoption greatly reduces burn-in time. Additionally, tests can be run with basic equipment that does not need high speed and high-level functions, reducing the costs associated with equipment manufacture. As a result, when peripheral costs are omitted, compared to our package burn-in equipment, the Tabai Espec WLBI equipment can be test calculated as processing 26 times the volume and 17.8 times more effective investment.

Table 1 Comparing package burn-in equipment and WLBI equipment for processing quantity and investment effectiveness

Equipment name	Package burn-in equipment MBI (Monitor Burn-In) System	Wafer Level Burn-in WBD-03 device for WLBI
Object device	64 Mb SDRAM TSOP-II 48-pin	64 Mb SDRAM
Equipment processing capacity	150 DUT/BIB, 64 BIB, 9,600 DUT	520 Die/wafer, 4 step/wafer 30 sec. (25 sec. burn-in + 5 sec. set-up) per step
Burn-in time	24 hours	30 × 4 + 60 (wafer transfer time) = 180 sec./wafer
Monthly processing quantity	150 × 64 × 30d × 24h / 24h = 288,000 DUT	30d × 24h × 3,600s/180s = 14,400 wafers 14,400 × 520 = 7,488,000 die
Processing volume ratio	1	26 times
Equipment cost comparison	MBI main unit: 25 million yen BIB 250 thousand yen × 64 = 16 million yen Total: 41 million yen	WBD-03 main unit: 35 million yen Prober: 20 million yen Probe card: 5 million yen Total: 60 million yen
Investment effectiveness	1	17.8 times

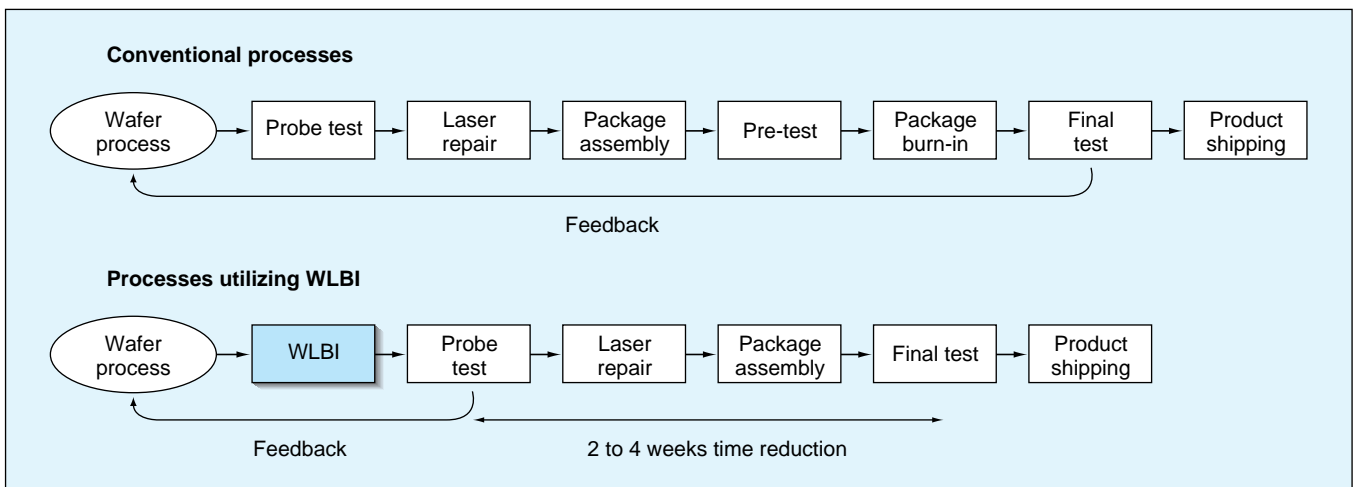


Fig. 2 Processes utilizing WLBI

(3) Improving yield

Fig. 2 shows processes adopting WLBI.

After package burn-in, repairs cannot be made to improve yield, but after WLBI burn-in wafer tests can be run, making repair possible.

Also, defect information feedback can be made to wafer processes 2 to 4 weeks sooner with WLBI than with package burn-in, speeding up process improvement. This method can serve as one means of meeting the recent demand for shorter time periods in device development.

(4) Guaranteeing KGD

Methods such as CSP and bare chip require special expensive sockets, and handling is difficult. With WLBI, though, contact can be made directly with the wafers, providing ease of burn-in, and performing probe tests to confirm quality at the next process can guarantee KGD.

3. Trends in WLBI equipment

3-1 The WLBI method

WLBI can be done using either the bundled contact method, in which contact is made with the entire surface of the wafers as one bundle, or using the partition contact method, in which multiple scans and contact are made.

Table 2 shows a comparative summary of the two contact methods.

Table 2 Bundled contact vs. partition contact

Item	WLBI	
	Bundled contact method	Partition contact method
Manufacturer	Companies "A" and "B"	Tabai Espec
Summary	Wafers are placed in a cassette as 1 bundle for burn-in	As with the probe tester, scanning is done, then burn-in
Use	Application beginning on mass production lines	Already applied to mass production lines
Equipment cost	Very expensive	Inexpensive
Contactors	Bump, and others	Vertical needle, and others
BIST	Unnecessary	Required
Testing	Possible	Using BIST
Mask function during test	Individual die masking not possible	Easily done
B/hour	24 to 96 hours	3 to 10 min./wafer
Handling 300 mmφ wafers	Both technology and costs make it difficult	Possible

3-2 Features of the bundled contact method

The bundled contact method has been proposed by several companies that have developed contactors that had previously been deemed technically impossible. The burn-in testing time and test contents for this method are the same as those done following conventional package burn-in. This method enjoys the distinct advantage of being able to utilize established testing technology and evaluation technology without modification. The method can also use current technology to perform burn-in for logic systems, for which it is difficult to incorporate BIST.

Merging test burn-in functions with the bundled contact method WLBI makes it possible to reduce the number of testers by transferring test items, cutting test costs with large volume processing. The market bears great expectations for this method as an ideal form of WLBI.

However, two major problems stand in the way of adopting the method.

First, the method requires over 10 thousand contactors for all the wafer surfaces, necessitating further improvements to achieve a higher level of contact reliability for the contactors. The technological hurdle becomes even greater when handling 300 mmφ wafers, due to a further increase in the number of contactors.

Second, not only must the high cost of a single unit at hundreds of millions of yen be reduced, the contactor running costs must be reduced as well. Currently, the

market evaluates the technology as having difficulty attaining cost competitiveness if conventional burn-in equipment is simply replaced with WLBI.

3-3 Features of the partition contact method

On the other hand, several companies have also proposed the partition contact method. Tabai Espec has adopted this method, introducing the approach for mass production processes in 1998. At present, we can state that the method is a very practical means of adopting WLBI.

Just as with the probe tester, this method comprises the burn-in tester, the prober, and the probe card, and burn-in is done while making contact with a number of chips simultaneously, and then the surface of all the wafers are tested by scanning. This method is based on the premise of having BIST built into the chips to reduce burn-in time. Burn-in time is cut to less than a minute, and 6 contactors are required for each chip.

Since the driving functions can be efficiently concentrated in BIST inside the chip, the unit is able to attain cost effectiveness. In addition to effectively reducing burn-in time, test costs are also shaved.

3-4 Basic differences between the bundled method and the partition method

The bundled contact method can be applied to devices when wishing to use the same test technology set up for package burn-in. Given the very high cost of modern equipment, this method could be considered for devices with high unit prices, as well as those requiring strict quality assurance, such as car electronics. Aligning the contactors and the wafers takes time, and so the method is not suitable for tests that take less than an hour.

The partition contact method can only be applied to devices which utilize the BIST technique of built-in testing. Therefore, the BIST technique is essential with conventional test technology for devices with excessive burn-in time and for equipment that is too complicated to allow ease of testing. When burn-in time is under 5 seconds, use of selection branches such as probe testers and idle testers may be considered.

Because wafers and contactors are in relatively close proximity in the bundled contact method, which uses contactors such as bump contactors*4, this method is not well suited to devices that generate high levels of heat. Since the partition contact method uses the same needle as the tester, this method is capable of handling devices that generate high levels of heat.

4. The current status of WLBI equipment

In 1995, Tabai Espec developed WBD-01 as a WLBI evaluation device for the partition contact method. Then in 1997, we developed WBD-02, adding DRAM mass production line functions to the equipment and giving it the capacity to handle 64 die for simultaneous burn-in.

In 2000, we produced the third-generation model WBD-03, which has the capacity for simultaneous burn-in of 256 die. This equipment has 4 times the processing capacity, but cost, footprint, and energy consumption are each increased only 1.4 times, offering an environmentally friendly design with considerable savings in cost, floor space, and energy. These small footprint models utilize new technology such as high-speed driver ICs, power circuits with high conversion efficiency, and automatic measurement circuits. Photo 1 shows a frontal view of the system, Table 3 gives basic specifications, and Fig. 3 shows a block graph of the system.

The development concept is based on improving burn-in efficiency and expanding the number of burn-in devices being tested by increasing the simultaneous processing capacity.

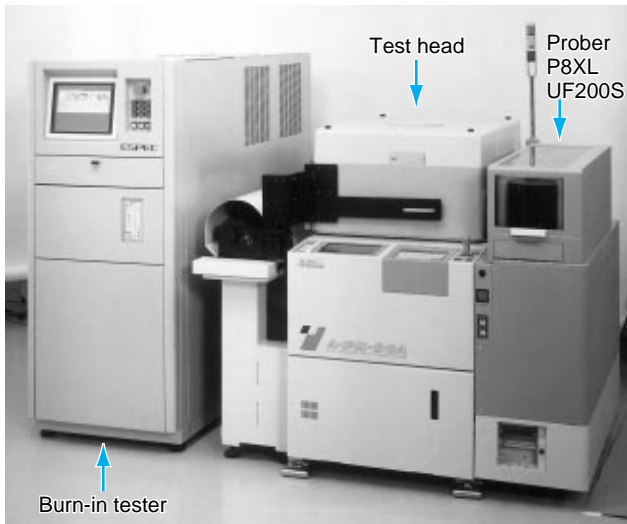


Photo 1 Frontal view of system

Table 3 Basic specifications for WBD-03

Item	Specifications
Maximum test cycle	10 MHz
Power supply	1 or 2 ch/die
Voltage	1 to 8 V (max. 20 V)
Current	150 mA/die (max. 400 mA)
Current measurement	0 to 200 mA/1mA
No. of drivers	8 or 16 ch/die
Driver voltage	V _{IH} 1 to 7 V/V _{IL} , -2 to 0 V, 0 to 4 V
Device output voltage measurement	0 to 10 V
OCP and OVP clock error detection for each die	Possible
Vector memory	Max. 4 MW
Simultaneous measurement quantity	Max. 256 die
Compatible prober	P8XL (TEL) / UF200S (TSK)

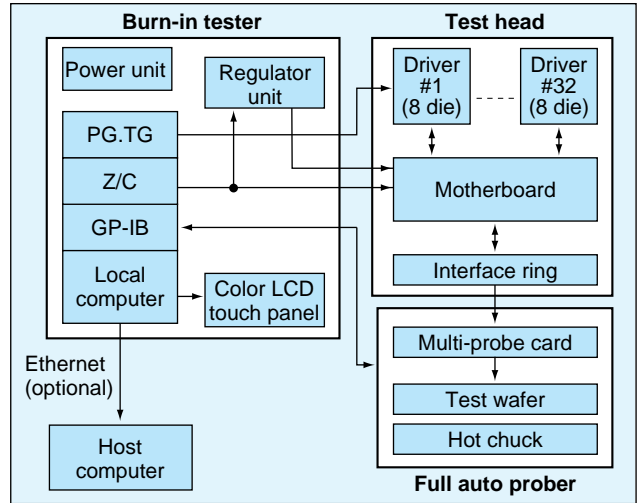


Fig. 3 System block graph

4-1 Main features of WBD-03

(1) Simultaneous burn-in of 256 die

This unit can complete all burn-in testing of normal 200 mmφ wafers in four scans. This performance capacity offers a major reduction in test time over 64-die processing, which requires 12 scans. Completing 200 mmφ wafers in 4 scans requires a 100 mm square contact area, but contact reliability evaluation has been completed for the perpendicular method needle, and targets have been set for starting up assembly line operation.

(2) Independent power source and drivers for each die

When a die defect occurs during burn-in, the defective die alone can be isolated from stress impression, and by doing so prevent any bad effects of the defective die from interfering with other good die. This ability eliminates the need for pre-testing the wafers directly after the production process, providing the advantage of greater process efficiency.

(3) Contact check capacity

The unit automatically determines whether the clock driver probes are in proper contact with the wafer pads, eliminating lack of burn-in due to contact defects.

As Fig. 4 shows, proper contact can be confirmed by detecting voltage V_f of the parasitic diode formed in the wafer manufacturing process. This function can also determine short or open circuit defects. Multiple pads may be used, such as power application pads and ground pads, but these pads cannot be checked in the same way as the signal pad. As a result, the function determines proper contact if the measured current is within the expected range.

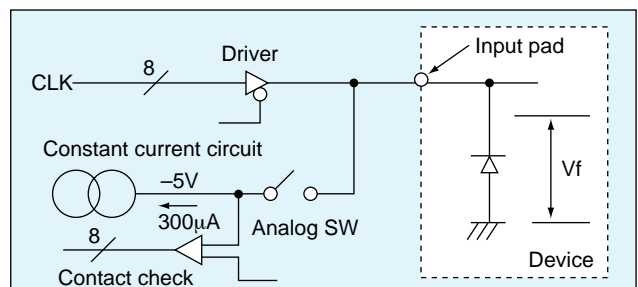


Fig. 4 Contact check circuit

(4) Monitoring function

Since the test results can be monitored with the BIST circuits, this function can be used to monitor burn-in. This capacity assures test reliability and provides the ability to determine pass/fail for each die independently. Strobe signals are used to compare all clock signals to expected values, and voltage can be measured with analog meters as well. Test results can also be output by category.

Fig. 5 shows a mapped display of test results, and Fig. 6 shows current measurement display results.

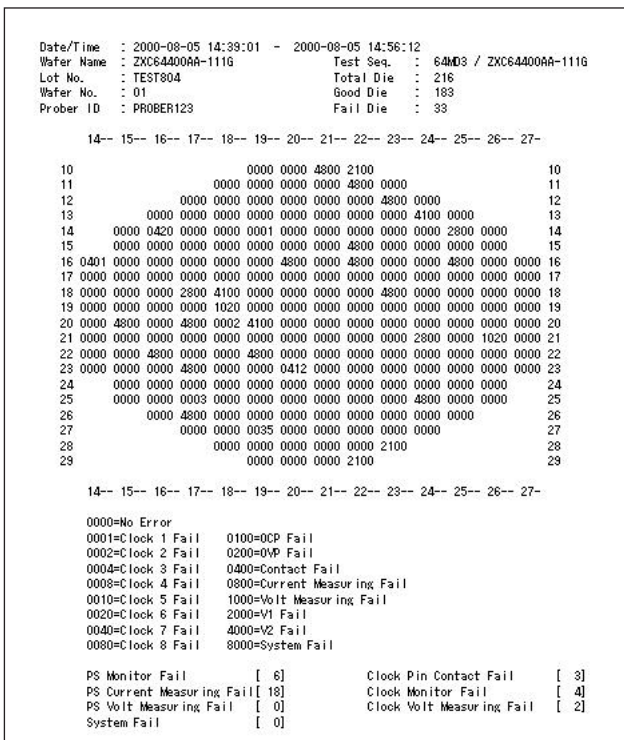


Fig. 5 Mapped display of test results

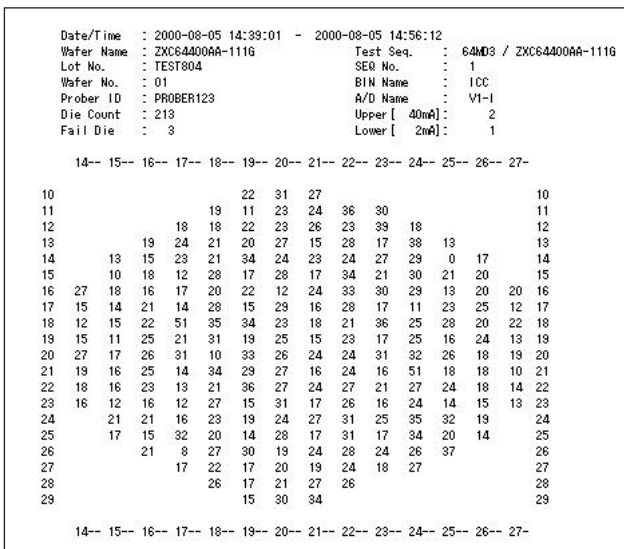


Fig. 6 Current measurement display

(5) JTAG*5 capability

In logic devices, tests are performed with methods such as scan passes and JTAG. This model has such functions as the ability to perform tests using vector data with maximum 4 MW vector calculation, and the ability to set input and output for each signal.

(6) Enhanced self-diagnosis functions

Along with the popularization of the ISO9000 Series has come increasing demand for traceability test equipment. Performing weekly and monthly equipment diagnosis requires the built-in capacity for self-diagnosis that can be done quickly in a simple operation. Studies on diagnostic methods were done at the design stage for this model, which is now provided with built-in diagnostic circuits. This eliminates the need for special diagnostic boards, and enables anyone to easily perform the diagnosis in a mere 3 minutes.

This model further assures test reliability during testing in such ways as dynamic monitoring of signal output, overload current, and output voltage range.

The most recent 10 files of diagnostic results are stored to provide administrative history.

(7) 300 mmφ wafer capacity

The 300 mmφ wafer size does not present a problem for the partition method, because a single wafer can be handled with multiple scans.

4-2 WLBI test technology

The current trend for more and more of total chip costs to be represented by test costs has become impossible to ignore. Current test technology very obviously cannot continue its rapid upward pace of improvements. It has become absolutely vital to introduce technology that builds tests into the chips, such as the BIST burn-in circuits.

(1) DRAM test technology

In DRAM, cell defects control testing. The BIST circuits that simultaneously select Word Line*6 (shown in Fig. 7. See next page.) have been installed as a method of efficiently applying stress to the cells, and these circuits have been established as a technology that can dramatically reduce burn-in time.

Even expanding the memory capacity will not increase the size of these BIST test circuits. BIST circuits have been studied as a means of handling peripheral circuits such as decoders as well, but this has not yet been established as the standard method.

(2) Flash memory test technology

For flash memory, hopes are high for transferring the E/W cycle test that requires so much time for the tester. Hopes are also high for Bad Block Management*7 with types such as AND and NAND, and WBD-03 has incorporated Bad Block Management capacity into its design. There is a trend toward incorporating into WLBI such functions as expanded application range of flash memory and to use stack memory to guarantee KGD.

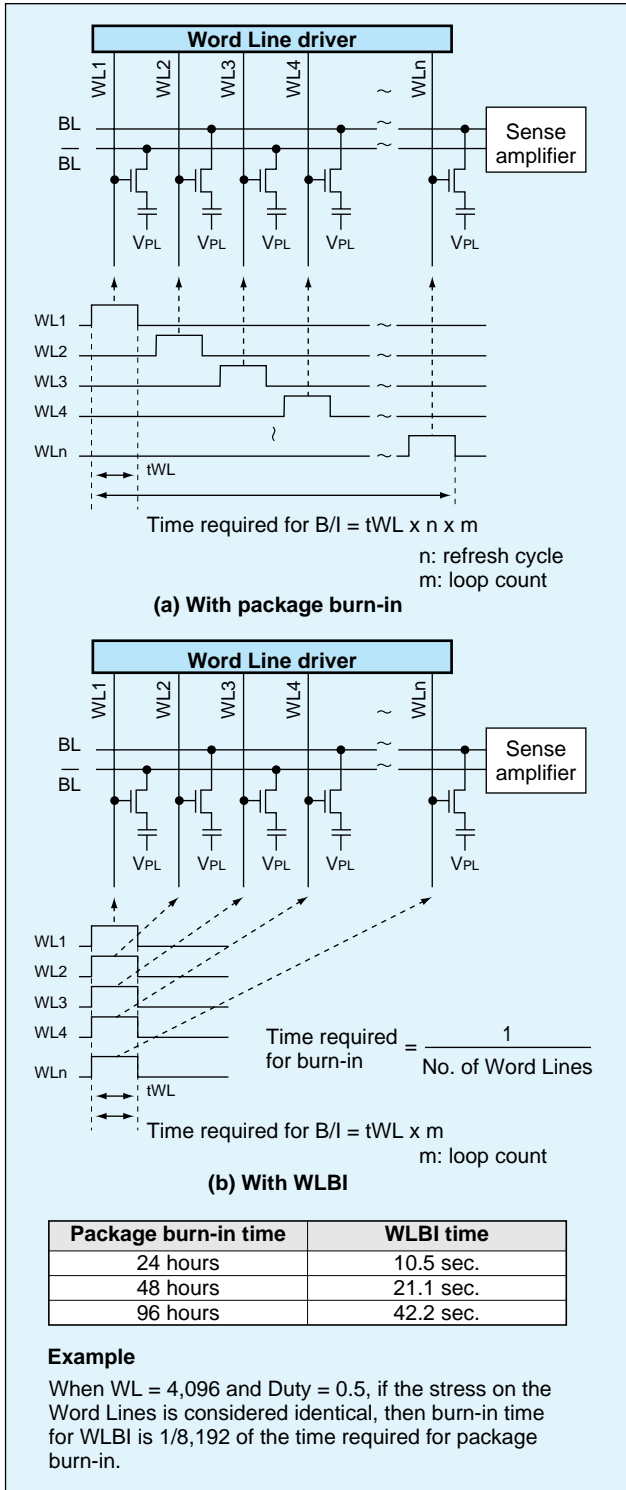


Fig. 7 DRAM test technology

(3) SRAM test technology

The adoption of WLBI in SRAM processes is becoming accepted as a means of guaranteeing KGD for such uses as stack memory. Unlike with DRAM, bundled stress application is not feasible with SRAM, and monitored burn-in is being done using BIST circuits as shown in Fig. 8.

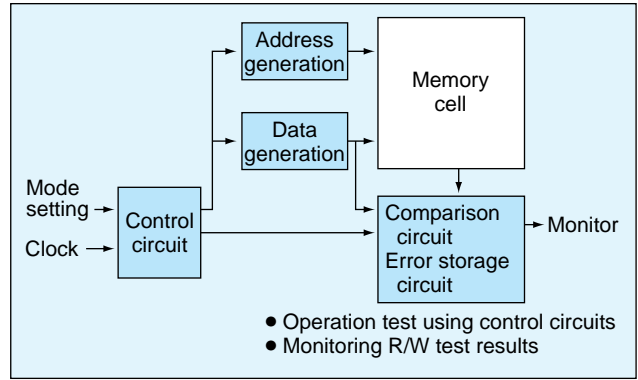


Fig. 8 SRAM test technology

(4) System LSI test technology

Individual circuits differ on logic system ICs, and so unified test circuits are not feasible. The efficient use of measures such as scan pass and JTAG with miniaturized BIST is being studied, but procedures with a wide application range have not yet been found, although it is hoped that this test technology will be established as soon as possible.

Fig. 9 shows an approach with System LSI test technology using JTAG.

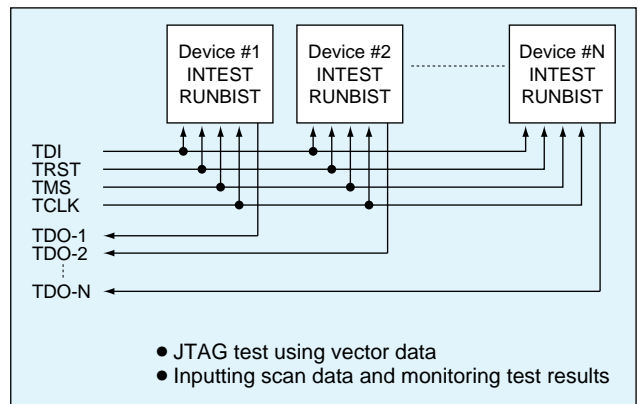


Fig. 9 System LSI test technology

Semiconductor design manufacturers are aware of the necessity for DFT (Designing Foolproof Tests) with chip design considering test methods in advance, but they are also aware of the importance of burn-in. When new methods appear, they will be linked to the discrimination of semiconductor manufacturers.

4-3 Examples of WLBI operation

WLBI operation has progressed beyond the initial stages in mass production lines turning out memory such as DRAM and SRAM. With flash memory and logic devices as well, the method has become well established.

In general the burn-in time is from 20 to 120 seconds, and the operating temperature is from 90°C to 125°C. The usual number of needles is 6 per die, but sometimes this can be as low as 2 per die. Needles are expensive, and items can wear out, and so during the design stage for BIST circuits every effort is made to minimize the number of needles required for burn-in tests.

Also during the design stage, the scan layout and the number of bundled die processed are optimized to perform burn-in with the minimum possible number of scans, as a means of effectively reducing operating costs.

Monitored burn-in is also becoming a more common means of testing, for example, while measuring voltage and current and determining test results.

4-4 Trends in probe card technology

To achieve bundled contact for the maximum 256 die, the contact area had to be expanded. A 100 mm square contact area is needed to perform tests covering the entire surface of 200 mmφ wafers in 4 shots.

When a wide contact area and a large number of vertical needles are required, a perpendicular card must be used because the relatively inexpensive horizontal method cantilever cannot be employed with vertical needles.

The perpendicular card has even been used successfully with the probe tester, but these results have not equaled the reliability attained from using a 100 mm square wide contact area.

To maintain the increased reliability necessary, we have requested technology development from the Japan Electronic Materials Corporation and the Tokyo Cathode Laboratory Co., Ltd., two companies that have achieved excellent results with perpendicular probe cards. Some of our customers have already begun operations using this new technology on mass production lines.

Photo 2 shows a Japan Electronic Materials Corporation perpendicular probe card (VCPC), and Photo 3 shows a Tokyo Cathode Laboratory Co., Ltd. perpendicular probe card (COBRA).

Photo 4 shows a probe card manufactured using a universal PCB developed by Tabai Espec. This universal PCB was developed to facilitate the low-cost manufacture of probe cards within a short time period. The universal probe cards have pads to provide contact to the test heads in the periphery of the PCBs. These pads are able to efficiently contact the probe needles.

This arrangement is not feasible when using a large number of vertical needles and wiring or when there are a large number of high-speed signals, but the method offers great advantages when it can be applied.

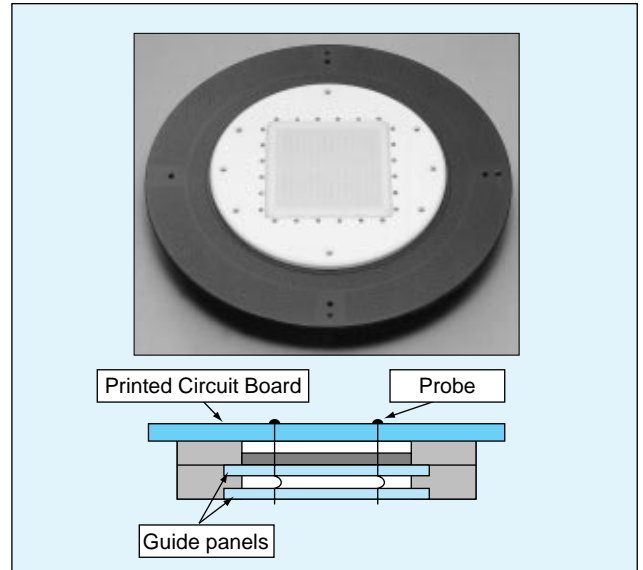


Photo 2 Perpendicular probe card
(VCPC: produced by Japan Electronic Materials Corporation)

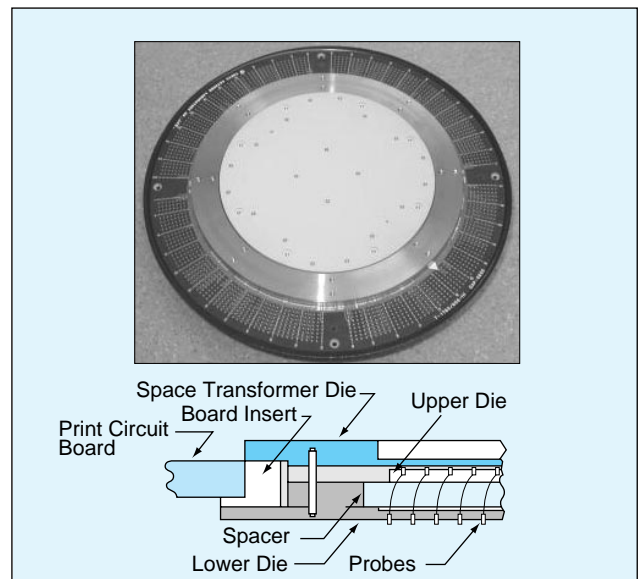


Photo 3 Perpendicular probe card
(COBRA: produced by Tokyo Cathode Laboratory Co., Ltd.)

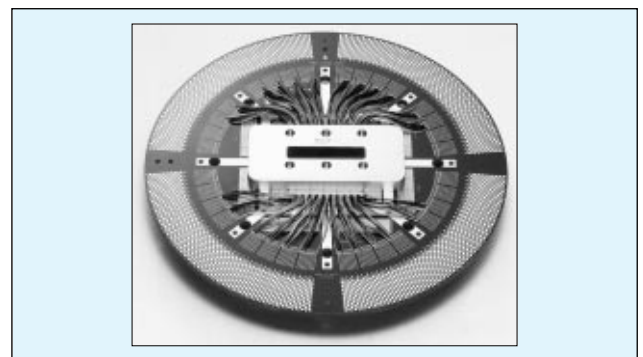


Photo 4 Universal probe card (produced by Tabai Espec)

5. Conclusion

Wafer level burn-in is regarded as an extremely effective approach for supplying KGD and reducing test costs, and studies are being undertaken to actively promote the use of this method. We at Tabai Espec are happy to hear your ideas on every aspect of this matter, and we will continue to spare no effort to contribute to the establishment of test technology improvement aiming toward an expanded range of applications for wafer level burn-in.

Establishing and developing WLBI test technology has not been possible to achieve through the efforts of device manufacturers alone. This must be done through mutual cooperation and understanding between semiconductor manufacturers and device manufacturers.

Terminology

***1 CSP**

Chip Size Package. An IC package that enables high-density packaging. This is a surface package type using BGA construction, the same or equivalent size as semiconductor chips.

BGA: Ball Grid Array. An IC package that enables high-density packaging. This is a surface package type with ball-shaped solder arranged in a lattice on the rear surface of a package to provide contact terminal with the PCB.

***2 Bare Chip Package**

The IC chip is connected directly to the PCB without using a package.

***3 MCP**

Multi Chip Package. Multiple chips are placed in a single package.

***4 Bump**

Connection electrodes formed on a wiring sheet and projecting out. These electrodes connect the wafer and the tester.

***5 JTAG**

Joint Test Action Group. An international group formed to standardize the testing of LSI and electronics devices.

***6 Word Line**

With DRAM, Word Line (WL) and Bit Line (BL) are used to select the cell intersect points.

***7 Bad Block Management**

Managing defective blocks in flash memory.

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