
Understanding the Technology 2

Nonvolatile memory: trends and evaluation equipment

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Portable data terminals are currently seeing a rapid surge in applications for such areas as PDAs (Personal Digital Assistants), and are also being used in expanding the data infrastructure. These trends are fueling competition among semiconductor manufacturers. Nonvolatile memory, which is capable of retaining data in memory when the power has been shut off, is generating particularly strong interest, and a wide range of nonvolatile memory is being developed. Requirements for equipment to test nonvolatile memory include high throughput speed and highly flexible evaluation functions. Espec produces a full line-up of test and inspection equipment for nonvolatile memory to meet the entire gamut of customer needs, from research and development through mass production. I would like to take this opportunity to introduce our line-up.

1. Introduction

Applications for portable data equipment are becoming widespread, and in this field nonvolatile memory is generating particularly strong interest. Pre-eminent among applications of nonvolatile memory are flash memory cell structures. A wide variety of proposals for new types of cell structures are focusing on these flash memory cell structures, with such aims as converting to MONOS cell structure*¹ to produce a simplified cell structure at lower cost, creating technology with multilevel applications, and providing high-speed writing capacity for mass production.

Competition is also heating up in the development of nonvolatile memory other than flash memory, such as FeRAM, MRAM, and OUM.

A test known as TDDB (Time Dependent Dielectric Breakdown) is required for FeRAM, due to the use of a new material known as High-K*². Evaluation of nonvolatile memory requires other tests as well, such as data retention tests, endurance tests to evaluate how many times the memory can be rewritten, and disturbance tests to check for errors in writing data. These basic evaluations are currently done using individual testers, but a far better solution would be low-cost evaluation equipment capable of multiple evaluations to be used in quality control.

The Espec line-up of nonvolatile test equipment includes equipment for evaluating raw material at the research and development stage, evaluation and test equipment with multi-functional high-speed processing capability for quality control, and equipment for inspecting high-volume devices.

2. Trends in nonvolatile memory

Nonvolatile memory does not require power to remain on to maintain device status, and so energy consumption can be reduced by shutting the device off when not in use. This approach is not only more environmentally friendly, it also greatly expands the potential range of application. This increases prospects for greater market scale by improving device utility in such ways as attaining instant-on capacity for computers. In addition, ease of integrated mounting with logic circuits can substantially improve performance by combining functions on a single chip. When memory can communicate with the digital signal processor (DSP) and the microprocessor on the same chip, broadband and high performance are brought within reach. Integrating memory on the chip can also reduce power requirements and power consumption. As a result of these factors, it has been reported the MIPS value per 1 μ W can be improved 3 to 5 times. If nonvolatile forms of memory can achieve average DRAM cost and performance, they will generate an enormous market in excess of 4 trillion yen.

Conventional nonvolatile memory used in semiconductors includes MROM, PROM, UV-EPROM, and EEPROM. These types of memory have limited application due to their inability to meet market needs in such areas as TAT (turn-around time), high-speed operation, low cost, and high capacity.

In recent years, the low cost and high capacity achieved by flash memory have driven a rapid market expansion in such applications as cellular phones, digital cameras, digital audio recorders, and MP3 music recorders. This trend has fueled expectations for further improvements in the functionality and performance of portable equipment, with interest focusing on nonvolatile memory as the key component.

The most sought-after capabilities in nonvolatile memory include low cost, high capacity, high-speed access, rewrite endurance, low power consumption, and ease of integration with logic circuits. Table 1 presents a comparison of the functions of the different types of memory.

Table 1 Comparison of functions for memory types

	Nonvolatile memory		
	Flash memory	FeRAM	MRAM
Read	Mid- / high-speed	Mid-speed	High-speed
Write	Low speed	Mid-speed	High-speed
Nonvolatile	Yes	Mid-term	Yes
Refresh	Not required	Not required	Not required
Cell surface area	4 to 8F ²	20F ²	20F ²
Integration level	Potential for multi-level technologies	Poor	Great potential
Rewrite capacity	10 ⁵⁻⁶	10 ¹²⁻¹⁵	10 ¹⁵
Integrated mounting with logic circuits	Complex → improvement with MONOS	Yes	Yes
Energy-conserving operation	No	Limited	Yes
Current	10 to 100 mA	Min. 10 mA	Min. 10 mA
Applied uses	Yes	Low capacity only	Under development
Manufacturers researching and producing	Fujitsu, Hitachi, Toshiba, Mitsubishi, Sharp, Samsung, Intel, AMD	Fujitsu, Hitachi, Toshiba, Panasonic, Rohm, Samsung, Infineon, Ramtron, TI, Hynix	IBM, Infineon, Motorola, NEC, Samsung, HP

	Nonvolatile memory	Volatile memory	
	OUM	SRAM	DRAM
Read	High-speed	High-speed	Mid-speed
Write	High-speed	High-speed	Mid-speed
Nonvolatile	Yes	No	No
Refresh	Not required	Not required	Required
Cell surface area	10F ²	40F ²	10F ²
Integration level	Great potential	Poor	Approaching limit
Rewrite capacity	10 ¹³	Unlimited	Unlimited
Integrated mounting with logic circuits	Yes	Yes	Complex
Energy-conserving operation	Yes	Yes	Limited
Current	Min. 10 mA	10 to 80 mA	100 mA
Applied uses	Under development, for 2005	Yes	Yes
Manufacturers researching and producing	Intel, STMicroelectronics	NEC, Cypress, Toshiba, etc.	Ramtron, Hynix, Samsung, Infineon

(1) Flash memory

(a) What is flash memory?

Flash memory is a type of nonvolatile memory based on block erasure of electrically rewriteable EEPROM (electrically erasable and programmable read only memory). Because it has achieved low cost and high integration, this type of memory is being put to a wide range of uses.

As Fig.1 shows, flash memory cells are composed of MOS transistors constructed with compound gates: the control gate (CG), and the floating gate (FG), which is inserted between the CG and a silicon plate. The CG threshold voltage for initiating current flow into the memory cell varies depending on the amount of charge accumulated in the FG, and logical data can be stored in memory. When electrons are electrically injected into the FG, or after electrons have been emitted, the electrons are retained in the FG even when the power is cut off, and so the memory is nonvolatile.

Flash memory types differ according to cell configuration and the method of accumulating electrical charge. Table 2 shows a comparison of AND, NAND, and NOR flash memory types.

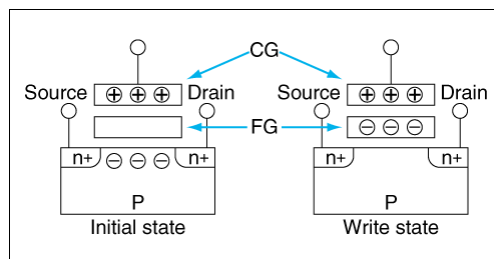


Fig.1 Data retention in flash memory

Table 2 Comparison of AND, NAND, and NOR flash memory types

	NOR	AND and NAND
Advantages	Fast random access	Fast write and erase
Disadvantages	Slow write and erase	Slow random access Can't write single bytes
Applications	Code memory applications Cell phones, games Rewriting conventional EPROM	File memory applications MP3 Digital cameras, videos

(b) NOR flash memory

The write operation (electron insertion) is performed using hot electrons (electrons that can cross the energy barrier from the silicon surface to the oxide film). The erase operation is performed using FN (Fowler Nordheim) current. Due to the large current used, write operations must be performed in single byte units.

The conventional use of NOR flash memory as PC BIOS storage memory and to replace EPROM as code storage memory is based on its random access capability. More recently, its application to cellular phones has been expanding rapidly.

Due to slow erase and write operations, improvement are being sought. The cell structure is also approaching its high-capacity limits, and so reforms of cell structure such as the MONOS cell structure are being considered.

(c) AND and NAND flash memory

Erase and write operations are both performed using FN current, and since the write current is small, multiple bytes can be written simultaneously. This type of memory does not have random access capability, but erase and write operations are fast, and high capacity is easy to attain. This type of memory is increasingly used in such file memory applications as music recording, digital still cameras, and as a replacement for small-capacity hard disks, but further reductions in cost would be desirable.

(2) MRAM

MRAM (magneto resistive random access memory) is attracting a lot of attention as a type of nonvolatile memory that has the potential for low-voltage operation, high rewrite endurance, and is comparable with DRAM in both high speed operation and high integration. MRAM uses a magnetic tunnel junction (MTJ) memory cell structure that manifests the tunneling magnet resistive (TMR) effect. This structure utilizes the principle that resistance increases according to the direction of magnetic flux. During the write operation, the level of resistance is controlled by the presence or absence of magnetic flux, and then the current during the read operation is determined as "1" or "0" depending on magnetic flux resistance.

TMR components^{*3} are easy to miniaturize, and both speed and rewrite endurance are expected to be comparable to DRAM. At present, this type of memory is still at the development stage with research focusing on materials and cell structure capable of increasing the MR ratio (amount of change in resistance). Applications are expected to be seen around the year 2005.

(3) FeRAM

As the DRAM capacitor has become miniaturized, the size of its accumulated charge has correspondingly decreased, and is now reaching its limits. Because of this, the so-called high-K materials with a high dielectric constant are garnering interest, and are believed to have potential for use as FeRAM. The hot topic at the current stage of this technology is the difficulty of miniaturizing the cell.

Games and memory cards are currently seen as possible applications for this memory.

(4) OUM (ovonic unified memory)

Applying the memory principle of optical disks to semiconductor memory has resulted in the development of OUM. By controlling the application of heat in the write operation, the resistance value varies due to the memory material changing between a crystalline and an amorphous state. The read operation then determines the value as "1" or "0" according to the change in current. The target date for applications using this memory is the year 2005.

3. Flash memory failure modes and evaluation technology

3-1 Endurance test

Data rewrite endurance testing determines how many times the write/erase operations can be repeated while still maintaining normal data. When electrical rewrite stress causes changes to occur in V_t , the threshold voltage of the cell, then the rewrite operation is no longer possible. This evaluation test can be classified in two categories.

(1) E/W (erase/write) cycle test

The number of times flash memory can be rewritten is on the order of 10^6 , but other types such as MRAM reach 10^{15} . Dummy time occurs in each cycle, greatly increasing test time, and so test equipment should ideally be capable of high-speed rewrite cycle tests to reduce lost time.

(2) Measuring operation time

Flash memory E/W operations are performed repeatedly until the control circuits within the device reach the specified threshold voltage (V_t).

Operation time increases in parallel to the course of cell degradation, which is caused by the number of charge operations. Measuring this E/W time makes it possible to grasp the degradation characteristics of the cell. Fig.2 shows an example of time measurement.

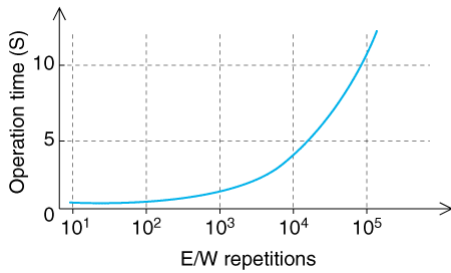


Fig.2 Example of time measurement for sector erase operation

3-2 Disturbance test

The E/W operations are performed by BL (bit line) or WL (word line) on the selected cells. However, when bias voltage is impressed onto cells other than those selected as connected to BL and WL, traps such as electron tunneling occur and cause changes in the threshold value V_t . This disturbance causes cells other than the selected cells to have their data mistakenly rewritten.

Using a device with a test mode that can externally control the impression voltage on WL and BL makes it possible to control the impression voltage and evaluate changes in data.

3-3 Measuring V_t distribution

Comparing the measured amount of charge stored in each cell with that of all cells makes it possible to grasp the level of deterioration of the cell. Using a device with a test mode that can externally control the comparative voltage of the sense amplifier, distribution can be measured by changing the comparative voltage and totaling up the number of bits that are changed from "0" to "1" as read in the data at each voltage level. Fig.3 shows an example of a V_t distribution measurement.

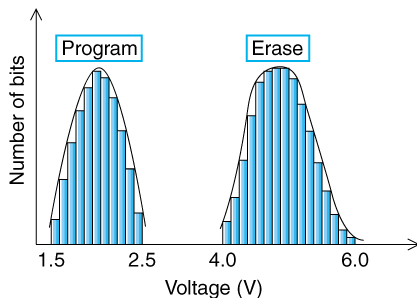


Fig.3 Example of V_t distribution measurement

3-4 Bad block control

The NAND and AND types of flash memory are capable of partitioning multiple blocks for E/W operations. However, to improve yield rate, if there is less than a specified number of bad blocks in the partition, the partition is judged as non-defective. These bad blocks will then be replaced with good blocks by the flash memory control software.

When the quality evaluation determines that the number of bad blocks exceeds the specified limit, a function must be available to imprint the quality information to the attribute area (alternative memory) for the bad blocks.

3-5 Excessive erasure

When electrons in the FG (floating gate) are emitted by FN (Fowler Nordheim current), an excessive emission can leave a positive hole (positive electrical charge) in the FG. This excessive emission results in changes in the threshold value V_t , making a correct write operation impossible.

3-6 Data retention

Electron loss from the FG causes changes in the data. Defects causing this loss include oxide films forming on the gate and FG electrification due to high voltage impression on the cell.

4. Test equipment

At this point, I would like to introduce some Espec equipment capable of testing nonvolatile memory.

4-1 Semiconductor parameter automatic evaluation system (AMM-1000: Photo 1)

At present, SiO_2 (silicon oxide film) is used as flash memory tunnel oxide film. The thickness of tunnel oxide film in processes less than $0.1\mu\text{m}$ is a maximum of 10\AA , and so the leak current for conventional silicon oxide film is too high and cannot be used. It is necessary to perform large-scale evaluation of new films with high dielectric constants to replace oxide films.

The AMM-1000 is capable of a maximum 200 channel bundled evaluation, achieving low-cost and high-speed TDDB (time dependent dielectric breakdown) evaluation.



Photo 1 TDDB evaluation system (Espec model AMM-1000)

4-2 Flash memory E/W cycle test equipment (RBM-F2)

Since the initial unit was developed in 1993, this model has incorporated evaluation technology for a full cross-section of flash memory, such as NAND, AND, NOR, SPI serial, I²C serial, all types of flash cards, and embedded types of memory. The model represents accumulated know-how based on its adoption by a wide range of companies.

When evaluating flash memory, endurance testing is used to measure E/W operation time and evaluate the degradation characteristics of cells. Distribution measurements are made for individual cell threshold values (V_t) for evaluating flash memory. In flash memory, the DFT (design for test) philosophy is incorporated from the outset. Setting test modes using commands and high-voltage impression enables the use of BIST (built-in self test) for ease of evaluation.

4-3 Flash memory test equipment (RBM-F3)

This monitoring burn-in equipment for mass production is our model for testing flash memory. The unit has high-speed test-monitoring capacity for NAND and AND memory, achieving simultaneous measurement of 16 pieces. Bad block control capability in the hardware makes high-speed processing a reality. The equipment also incorporates such features as imprint control and master ROM. Tests that take a lot of time with testers are shifted to the burn-in unit. Incorporating these types of functions and performance has lowered test costs.

4-4 Wafer burn-in equipment (WBD-03)

This equipment is being installed on mass-production lines for use with memory such as DRAM and SRAM. Application of this model to flash memory burn-in is continuing to expand. We can also expect to see this equipment used for bad block control.

There has been an increase in the use of custom-made equipment for stack type flash memory for portable equipment, and this has brought an upsurge in test costs. Trend indicators now point to a stronger shift toward wafer burn-in as a means of resolving this predicament. Photo 2 shows the WBD-03 system.

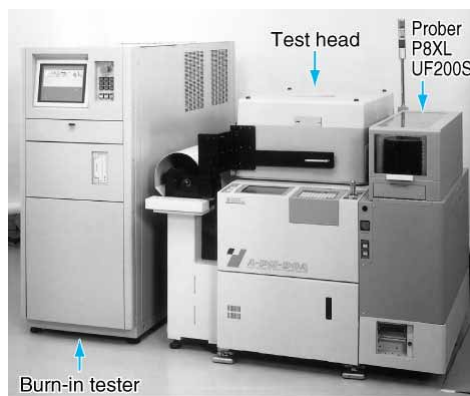


Photo 2 Water burn-in equipment (Espec model WBD-03)

5. Nonvolatile memory evaluation equipment (New product: RBM-F25 Series)

This equipment targets devices with integrated mounting of different types of memory, including nonvolatile memory such as FeRAM and flash memory and systems with logic devices such as LSI. These are monitoring burn-in systems that perform high-speed evaluation testing.

Photo 3 shows the appearance of the RBM-F25 system, and table 3 presents the basic specifications.



Photo 3 Nonvolatile memory evaluation equipment (Espec model RBM-F25)

Table 3 RBM-F25 basic specifications

Item	Specifications
Max. test cycles	10 MHz, 30 on-the-fly
Power source	2 (4 optional)
Voltage	1 to 10 V; 10A, 1 to 13 V; 5 A
No. of driver channels	114 ch (4 ch option); internal monitoring; 64 ch
Driver voltage	VIH: 1 to 6 V; VIHh: 1 to 13 V; 4 ch
OCP and OVP clock error detection	Yes
Vector memory	64 bit x standard 8 MW (W: 64 bit), max. 32 MW
No. of simultaneous measurements	8 / 4
Address generation	32 / 28
Data generation	16

When testing system LSI, tests are performed with various vector generating functions and clock signal generating functions, and test results can be determined using the monitoring function.

When testing flash memory using such functions as the high-speed bad block control function and the pattern generation function that can generate complex algorithms, this equipment can take over test functions that have been done by individual testers. The design of this test equipment has incorporated the concepts of expandability and flexibility to enable handling tests for FeRAM and MRAM as well as newly developed nonvolatile memory. Let's look at the features of this equipment.

(1) E/W cycle tests for various types of flash memory

This equipment can perform high-volume, high-speed E/W cycle tests on memory from various manufacturers and including various types of flash memory, such as AND, NAND, and NOR.

For RBM-F2 upward compatibility, it is possible to further increase evaluation test speed using the RBM-F25 and RBM-F2 burn-in boards and test programs.

The equipment offers efficient test capability using bad block control and Ready/Busy signal control functions. Also, using the master ROM function, the equipment can be used as a mass ROM writer to write data at the time of shipping.

(2) Various system LSI tests

System LSI monitoring burn-in tests can be run at high speed with large volume capacity using the maximum 32 MW vector data generation and monitoring functions.

This equipment incorporates both vector generator*4 and memory pattern generator*5 functions, which can be operated simultaneously, and the equipment can be used for testing devices that have integrated mounting of logic and memory.

Testing can be run at test cycles up to 10 MHz using the JTAG*6 function.

TOC operation data can be redirected using the master ROM function, and this equipment can accommodate BIST using the flexible vector data generation function. Fig.4 shows the devices that can be evaluated using this equipment.

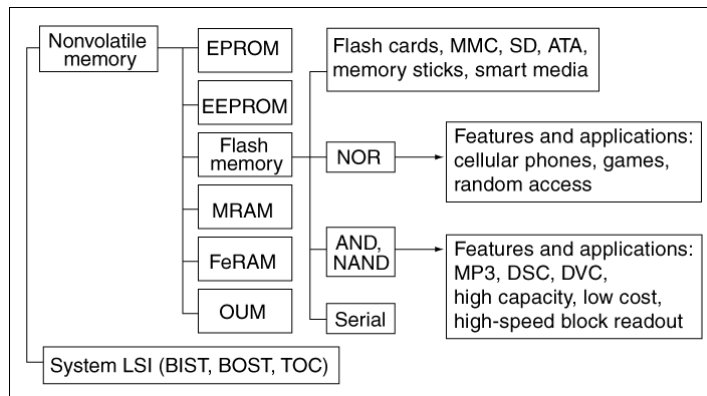


Fig.4 Devices evaluated

(3) Flexible structure

To enable handling devices with breakthrough technology, the equipment incorporates pattern generation and control functions for PG type PCBs and control functions for driver PCBs that can be upgraded in the field.

For driver PCBs, the equipment incorporates a highly-flexible 2 MB of work memory, which can be used to store evaluation test data. These attributes provide a flexible approach to evaluation testing for as yet undeveloped devices.

At present the equipment achieves high-speed operation using buffer control for such operations as bad block control, measuring E/W time, measuring Vt distribution, and counting failed bits.

(4) Evaluation tests and mass production tests

The RBM-F25 model uses a one-piece/one-zone configuration to attain high speed for various types of evaluation tests. The RBM-F25X uses an n-piece/one-zone configuration to handle mass production tests. Both operability and test program creation feature a high degree of flexibility that can handle testing from evaluation tests to mass production tests.

Fig.5 and Fig.6 show the system configuration.

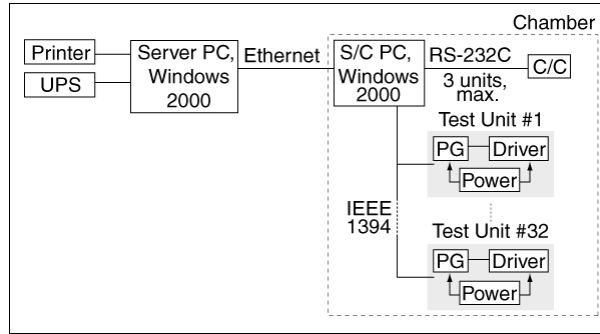


Fig.5 RBM-F25 system configuration for evaluation testing

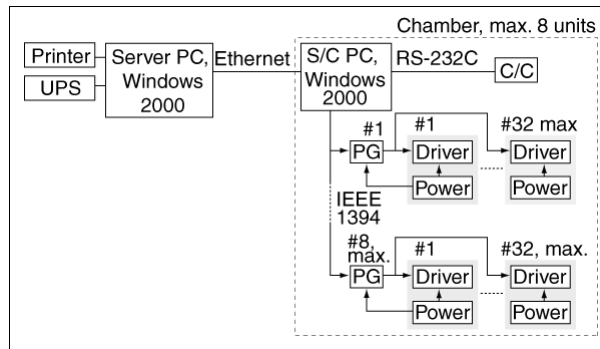


Fig.6 RBM-F25X system configuration for mass production testing

(5) Self-diagnosis function

Monitoring, memory check, wave form output, and voltage and current measurement for DUT power are possible without using a special self-diagnostics board. Periodic diagnosis can be achieved quickly and easily.

(6) Centralized control of the burn-in chamber

Up to 8 burn-in chambers can be controlled at a single host computer.

6. Conclusion

Flexible and high-speed evaluation equipment for nonvolatile memory is urgently required for devices such as PDAs, cell phones, and digital cameras. We at Espec are proud to offer equipment capable of high-speed processing of high-volume evaluation data. We are developing equipment with the flexibility and expandability to handle new functions as they arise. We shall continue to incorporate new advances into our equipment to meet all our customers' needs.

Terminology

*1. **MONOS structure (metal oxide nitride oxide silicon)**

As attempts have been made to miniaturize the FG (floating gate) structure, beyond a certain point defects occur and the limit of miniaturization has been reached. Because of this, attention has focused on the MONOS structure that alters the electrical charge accumulator section from FG to nitride film. Advantages include miniaturization of memory cells and elimination of production processes.

*2. **High-K**

This material has a high capacity for accumulating electrical charge. Dielectric memory materials include substances such as Y1 and PZT. The advantages of this material include both its ability to be miniaturized and its nonvolatility.

$$K = \frac{1}{4\pi\epsilon_0} \quad \epsilon_0 = \text{dielectric constant}$$

*3. **TMR components (tunneling magnet resistive)**

These components comprise an insulation film between two ferromagnetic layers. The film changes the resistance value by changing the direction of magnetic flux of one of the magnetic bodies. When write current is impressed, the amount of voltage is determined as "1" or "0". TMR components must have large variations in resistance value.

*4. **Vector generator**

This device generates random patterns for testing logic devices.

*5. **Memory pattern generator**

This device generates a variety of patterns to test memory devices.

*6. **JTAG (joint test action group)**

JTAG is made up of 4 control signals and 1 monitoring signal, and the internal resistor of the device is controlled with serial data to perform function testing. A pass/fail determination is rendered based on monitoring the test results. With the penetration of the BIST and DFT approach, this method is garnering attention.

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